MITSUBISHI

PROGRAMMABLE CONTROLLER

MELSEC-A

User's Manual

type A2ASCPU(S1)

MITSUBISHI ELECTRIC

REVISIONS

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INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

CONTENTS

1. GENERAL DESCRIPTION

This manual describes the performance, functions and handling instructions for the A2ASCPU and A2ASCPU-S1 general purpose programmable controllers (hereafter referred to as A2ASCPU), as well as the specifications and handling instructions for the memory cassettes, power supply modules and base units used in connection to the A2ASCPU.

The A2ASCPU, when compared with existing A1SCPU has improved performance and functions such as increased program capacity and I/O points and increased I/O device points.
Please make the best use of the performance and functions to efficiently use the A2ASCPU.

When existing programming units and software package are used, applicable ranges are limited according to the CPU type (PC type) to be used.
..... Refer to Section 1.3 for settings.

Refer to Section 2.2 for the equipment list of the units and modules that are compatible with the A2ASCPU.
Refer to Section 1.4 for the special function modules whose device ranges are limited.

Refer to each of the following manuals as necessary when using the A2ASCPU.

- ACPU Programming Manual (Fundamentals) IB-66249
- ACPU Programming Manual (Common Instructions) IB-66250
- AnACPU Programming Manual (Dedicated Instructions) IB-66251
- AnACPU Programming Manual (AD57 Instructions) IB-66257
- AnACPU Programming Manual (PID Instructions) IB-66258
- MELSECNET, /B Data link System Reference Manual IB-66350

1.1 Features

The A2ASCPU has the following features when compared with the A1SCPU:

(1) The program capacity and the number of inputs and outputs have been increased.

- Program capacity .....Max. 14K steps
- Number of inputs .....1024 points (when an A2ASCPU-S1 is used) and outputs

(2) The I/O device points, link device points and data register points have been increased.

- I/O device (X/Y) .....8192 points (X/Y0 to 1FFF)
- Link relay (B) .....8192 points (B0 to B1FFF)
- Link register (W) .....8192 points (W0 to W1FFF)
- Data register (D) .....8192 points (D0 to 8191)

(3) The A2ASCPU incorporates 64-Kbyte and 256-Kbyte RAM memory. RAM memory of 64 Kbytes (A2ASCPU) and 256 Kbytes (A2ASCPU-S1) is built in and backed up by battery.
An optional memory cassette (EPROM, EEPROM) can be installed to the A2ASCPU.

(4) Data communication requests can be batch-processed.

- By turning ON the M9029 by the sequence program, all data communication requests (from the AD51H-S3, AD57G-S3, AD51FD, AJ71UC24, A1SJ71C24-R2 (PRF/R4) and peripheral devices) received in a scan can be processed by one END processing.
- Batch processing of data communication requests eliminates delays in data communication with each module. (When the M9029 is OFF, the A2ASCPU processes only one request to one scan.)

(5) The operation processing speed (sequence instruction) has greatly been increased.
While the processing speed of the A1SCPU operating in the refresh mode is 1.0 μsec/step, that of the A2ASCPU is as high as twice.

(6) The A2ASCPU can execute AnACPU dedicated instructions. It can execute AnACPU dedicated instructions, AD57 instructions and PID control instructions.

1.2 Comparison of Performance Specifications Between the A2ASCPU and the A1SCPU

The following table makes a comparison of performance specifications between the A2ASCPU and the A1SCPU. Other items not included herein are the same as those of the A1SCPU.

Item \ CPU Type		A2ASCPU(S1)	A1SCPU
I/O control method		Refresh mode	Refresh mode/Direct mode selective
Processing speed (sequence instruction)(μsec/step)		0.2	Direct: 1.0 to 2.3 Refresh: 1.0
Number of instructions	Sequence instructions	22	26
	Basic and application instructions	239	235
	Dedicated instructions	200	0
Constant scan (msec)		10 to 190	—
Main program capacity		Max. 14K steps	Max. 8K steps
Memory capacity and memory cassette type	Memory capacity (built-in RAM)	64 Kbytes (256 Kbytes)*1	32 Kbytes
	EPROM type memory cassette	A2SMCA-14KP	A1SMCA-8KP
	EEPROM type memory cassette	A2SMCA-14KE	A1SMCA-2KE A1SMCA-8KE
Number of I/O points		512(1024)*1	256
Number of device points	Internal relay (M) (points)	7144	1000
	Link relay (B) (points)	4096	1024
	Link register (W) (points)	4096	1024
	Data register (D) (points)	6144	1024
	File register (R) (points)	8192	4096
	Annunciator (F) (points)	2048	256
	Timer (T) (points)	2048	256
	Counter (C) (points)	1024	256
	Index register (V,Z) (points)	14	2
Comment (points)		Max. 4032	Max. 1600
Extension comment (points)		Max. 3968	—
Watchdog timer setting		200 (msec) fixed	10 to 200 (ms)
Data link		MELSECNET(II)*2 MELSECNET/B	MELSECNET(II)*2 MELSECNET/B

*1 When an A2ASCPU-S1 is used.

*2 The MELSECNET (II) link module can be used by loading it to the A5[ ]B or A6[ ]B extension base unit.

POINTS

(1) Starting up the A2ASCPU with an existing system FD or peripheral device (programming unit) narrows the range of devices available. See Section 1.3.

(2) To use the sequence programs prepared for the A1SCPU with the A2ASCPU, see APPENDIX 2.

1.3 Restrictions When Using Conventional System FD or Peripheral Devices

When starting up the A2ASCPU by a conventional system FD (FDs indicate PC types "AnA" and "A3H") or peripheral devices (A7PU, A7PUS, A8PUE), the applicable device range is restricted.

Applicable device ranges and programming for devices outside the device ranges for a specific system FD and peripheral device are as given in the table below.

1.3.1 Usable device ranges

System FD, peripheral device / Item	AnA compatible (PC type: AnA)		A3H compatible (PC type: A3H)	
	SW4GP-GPPAEE, SW0IX-GPPAE, MELSEC-MEDOC	A8PUE	SW3GP-GPPAEE	A7PU/A7PUS
Instruction (Sequence, basic, application, dedicated)	All instructions can be used.			
Sequence program capacity	Main sequence program: Max. 14K steps			
I/O device points (X/Y)	Max. 2048 points (X/Y0 to 7FF)			
M, L and S relays	8192 points		2048 points	
Link relay (B)	4096 points (B0 to BFFF)		1024 points (B0 to B3FF)	
Timer (T)	2048 points (Default: 256 points)		256 points	
Counter (C)	1024 points (Default: 256 points)		256 points	
Data register (D)	6144 points (D0 to D6143)		1024 points (D0 to D1023)	
Link register (W)	4096 points (W0 to WFFF)		1024 points (W0 to W3FF)	
Annunciator (F)	2048 points (F0 to F2047)		256 points (F0 to F255)	
Index register (V, Z)	14 points (V, V_1 to V_6, Z, Z_1 to Z_6)		2 points (V, Z)	
Comment	Max. 4032 points		Max. 4032 points	
Extension comment	Max. 3968 points			
Latch (power failure compensation) range	L0 to L8191 can be latched.		L0 to L2048 can be latched.	
I/O assignment	Number of occupied I/O points and unit model can be entered.	Number of occupied I/O points can be entered.		

(1) Device ranges not mentioned in the table above are same as those for the A2ASCPU.
(2) For functions which can be controlled by peripheral devices, refer to the operating manual for the specific peripheral device.

POINTS

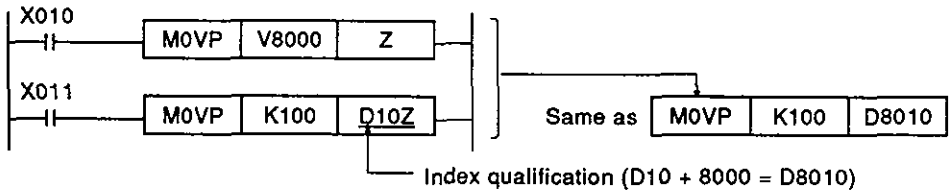
(1) When the system is started by an AnA compatible system FD, set the PC type to A2A for A2AS(S1). Operation must be within the AnACPU's range.
(2) When the system is started by an A3H compatible system FD, set the PC type to A3H for A2AS(S1). Operation must be within the A3HCPU's range.
(3) For compatibility of peripheral devices and system FDs (S/W package), refer to Appendix 1.

1.3.2 Programming with devices outside the applicable device range

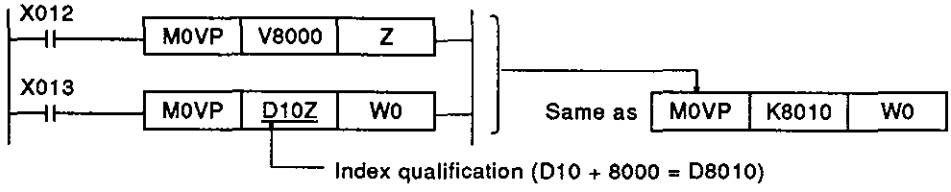
When the system is started up by using a system FD for AnA or A3H, devices outside the applicable device range can be used by specifying index qualification with the sequence program.

(1) Index qualification for devices

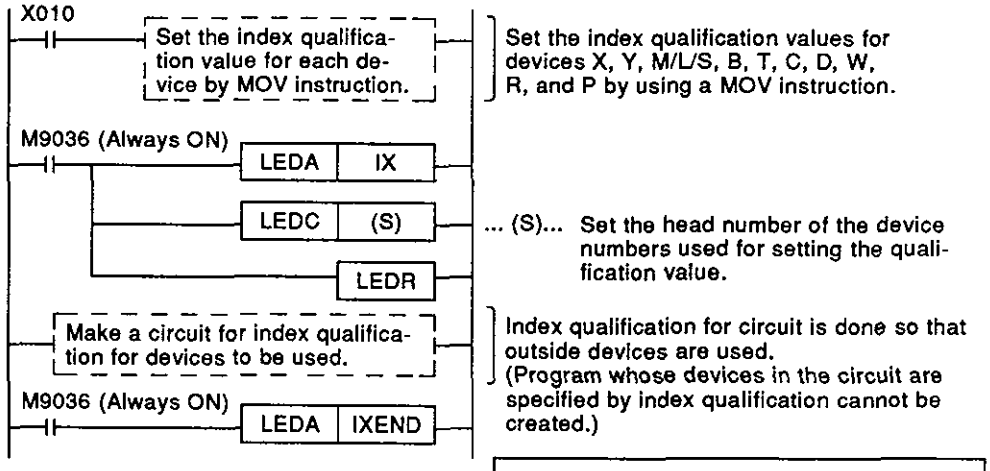
(a) A program example to write "100" to D8010:



(b) A program example to write D8010 data to link register W0:



(2) Index qualification for circuit



- Refer to the following manual for program creation:
  AnACPU Programming Manual (Dedicated Instructions)

POINTS

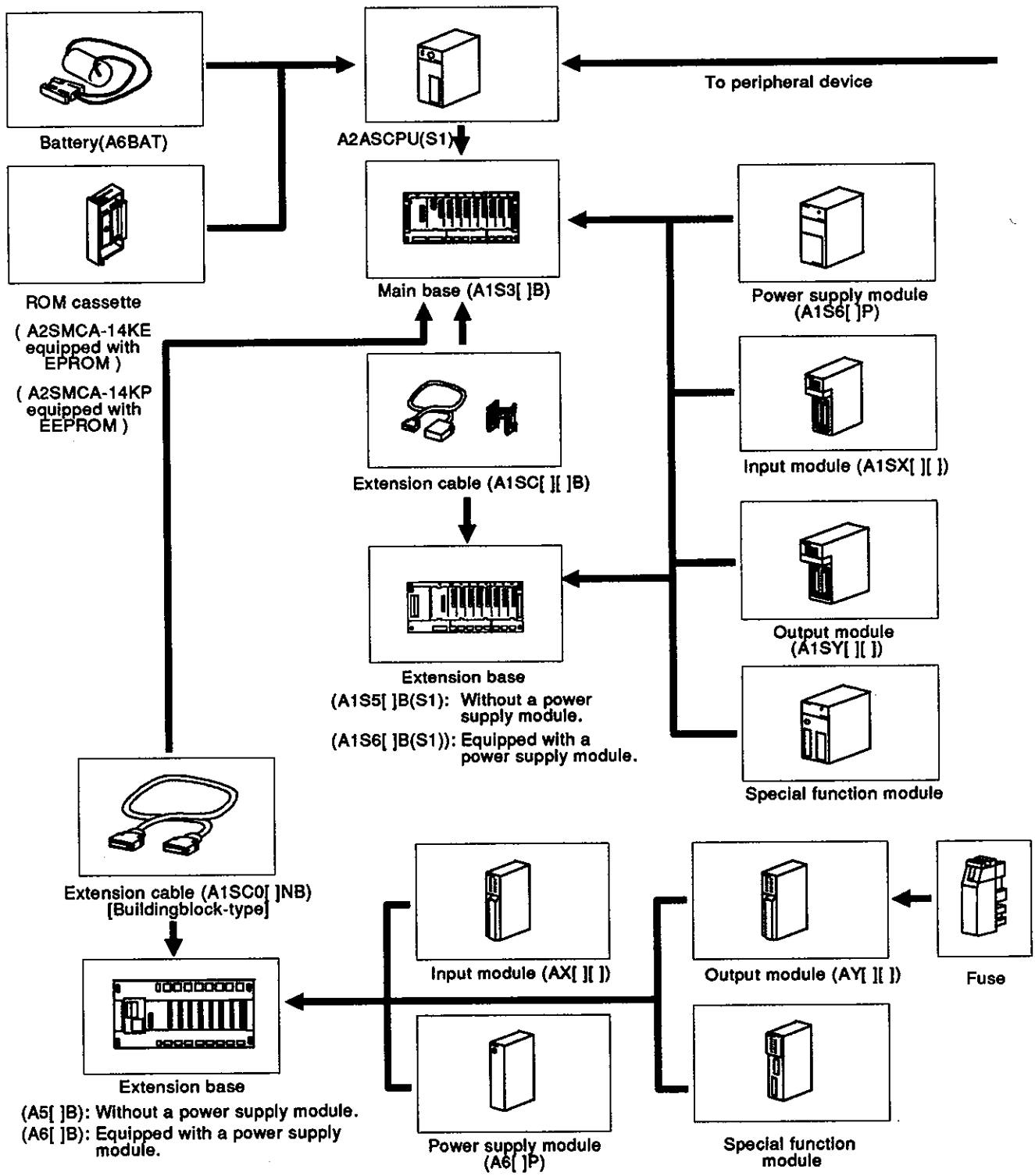
(1) When a system FD for the AnA is used, bit devices can be specified for index qualification.
(2) When a system FD for the A3H is used, extension timers and extension counters cannot be used. Bit devices (X, Y, M, L, S, and B) cannot be specified for index qualification.

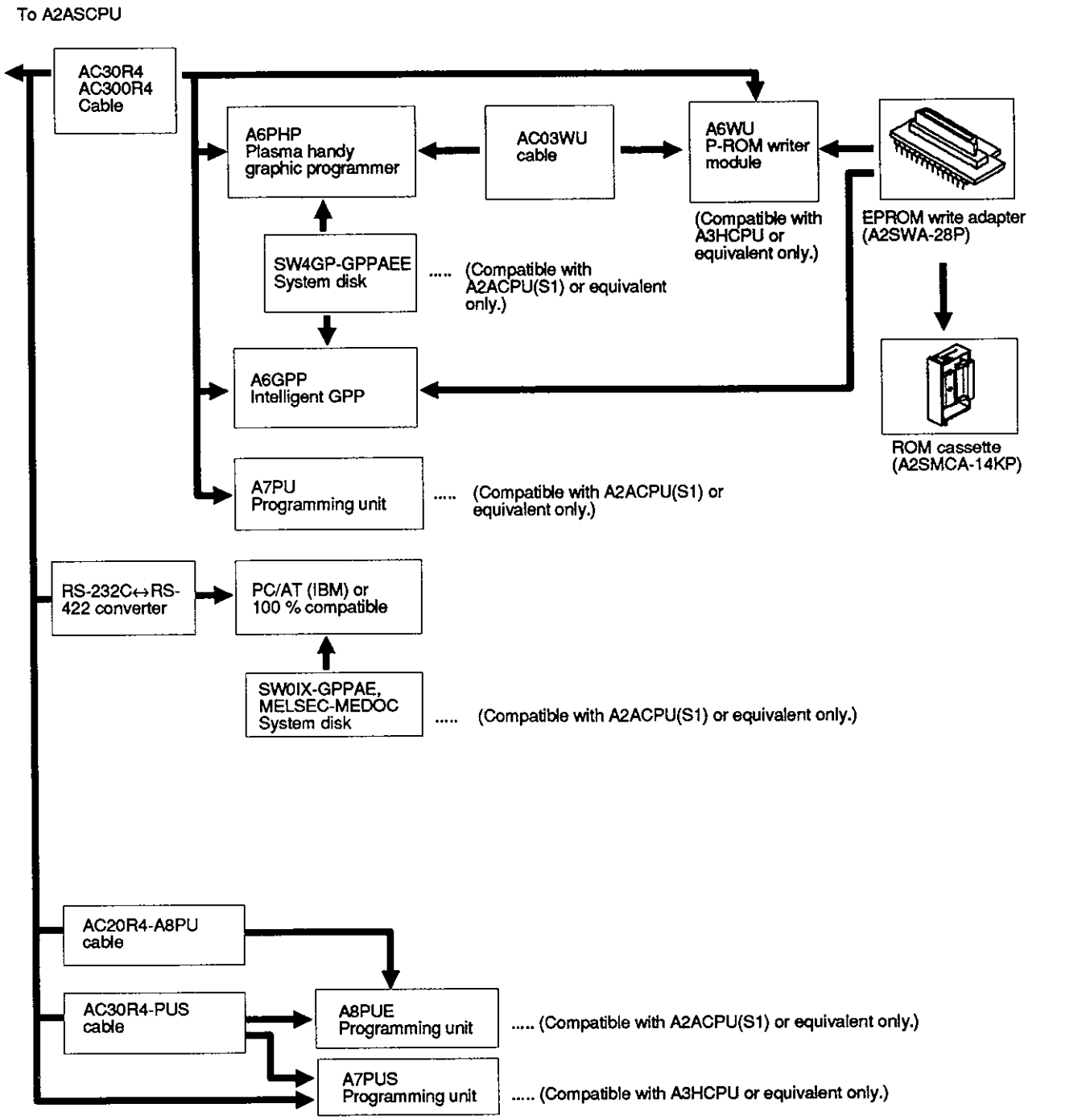
2. SYSTEM CONFIGURATION

This section describes the applicable system configuration, cautions on the system configuration, and component devices of the A2ASCPU.

2.1 Overall Configuration

The following figure shows a configuration when the A2ASCPU is used independently.





POINT

Refer to the Operating Manual of peripheral equipment to be used for applicable cable, printer and equipment.

2.2 System Equipment

The following table shows the system equipment consisting of various modules and devices which can be used.

Module	Model	Description		Number of Inputs/ Outputs	Current Consumption		Remarks	* Approved Standard
					DC5V(A)	DC24V(A)		
CPU module	A2ASCPU	Number of I/O points : 512 Memory capacity : 64 Kbytes		—	0.40	—	RAM memory embedded	UL/CSA
	A2ASCPU -S1	Number of I/O points : 1024 Memory capacity : 256 Kbytes		—	0.40	—		
Power supply module	A1S61P	5 VDC, 5 A	Input 100/200 VAC	—	—	—	Loaded to the slot for power supply of main base or extension base.	
	A1S62P	5 VDC, 3 A/24 VDC 0.6A						
	A1S63P	5 VDC, 5 A	Input 24 VDC					
Input module	A1SX10	16-input 100 VAC input module		16 [16 inputs]	0.05	—		UL/CSA
	A1SX20	16-input 200 VAC input module		16 [16 inputs]	0.05	—		
	A1SX30	16-input 12/24 VDC, 12/24 VAC input module		16 [16 inputs]	0.05	—		UL/CSA
	A1SX40	16-input 12/24 VDC input module		16 [16 inputs]	0.05	—		
	A1SX40-S1	16-input 24 VDC input module		16 [16 inputs]	0.05	—		
	A1SX40-S2	16-input 24 VDC input module		16 [16 inputs]	0.05	—		
	A1SX41	32-input 12/24 VDC input module		32 [32 inputs]	0.08	—		
	A1SX41-S2	32-input 24 VDC input module		32 [32 inputs]	0.08	—		
	A1SX42	64-input 12/24 VDC input module		64 [64 inputs]	0.09	—		
	A1SX42-S2	64-input 24 VDC input module		64 [64 inputs]	0.09	—		
	A1SX71	32-input 5/12 VDC input module		32 [32 inputs]	0.075	—		
	A1SX80	16-input 12/24 VDC sink/source input module		16 [16 inputs]	0.05	—		
	A1SX80-S1	16-input 24 VDC sink/source input module		16 [16 inputs]	0.05	—		
	A1SX80-S2	16-input 24 VDC input module		16 [16 inputs]	0.05	—		
	A1SX81	32-input 12/24 VDC sink/source input module		32 [32 inputs]	0.08	—		
	A1SX81-S2	32-input 24 VDC input module		32 [32 inputs]	0.08	—		

*: Class 2 power supply specified by the UL/CSA Standard must be used.

Module	Model	Description	Number of Inputs/ Outputs	Current Consumption		Remarks	* Approved Standard
				DC5V(A)	DC24V(A)		
Output module	A1SY10	16-output relay contact output module (2 A)	16 [16 outputs]	0.12	0.09		UL/CSA
	A1SY18A	8-point relay contact output module (2 A) All points independent	16 [16 outputs]	0.24	0.075		
	A1SY22	16-output triac output module (0.6 A)	16 [16 outputs]	0.27	(200 VAC) 0.004		UL/CSA
	A1SY28A	8-point triac output module (1 A) All points independent	16 [16 outputs]	0.11	—		
	A1SY40	16-output 12/24 VDC transistor output module (0.1 A) sink type	16 [16 outputs]	0.27	0.016		UL/CSA
	A1SY41	32-output 12/24 VDC transistor output module (0.1 A) sink type	32 [32 outputs]	0.50	0.016		
	A1SY42	64-output 12/24 VDC transistor output module (0.1 A) sink type	64 [64 outputs]	0.93	0.016		
	A1SY50	16-output 12/24 VDC transistor output module (0.5 A) sink type	16 [16 outputs]	0.12	0.12		
	A1SY60	16-output 24 VDC transistor output module (2 A) sink type	16 [16 outputs]	0.12	0.015		
	A1SY60E	16-output 12 VDC transistor output module (1 A) source type	16 [16 outputs]	0.20	0.01		
	A1SY68A	8-point 5/12/24/48 VDC transister output module sink/source typeAll points independent	16 [16 outputs]	0.13	—		
	A1SY71	32-output 5/12 VDC transistor output module (0.016 A) sink type	32 [32 outputs]	0.40	0.15		
	A1SY80	16-output 12/24 VDC transistor output module (0.8 A) source type	16 [16 outputs]	0.12	0.04		
	A1SY81	32-output 12/24 VDC transistor output module (0.1 A) source type	32 [32 outputs]	0.50	0.016		
Input/ output combi- nation module	A1SH42	32-input 12/24 VDC input module 32-output 12/24 VDC transistor output module (0.1 A) sink type	32 [32 inputs/ outputs]	0.50	0.008		
	A1SX 48Y18	8-input 24 VDC input module (sink type) 8-output relay contact output module (2 A)	16 [8 inputs/ outputs]	0.085	0.045		
	A1SX 48Y58	8-input 24 VDC input module (sink type) 8-output 12/24 VDC transistor output module (0.5 A)	16 [8 inputs/ outputs]	0.06	0.06		UL/CSA
Dynamic input module	A1S42X	16-, 32-, 48- and 64-point 12/24 VDC dynamic input module	Number of set points (Inputs [ ])	0.08	—		
Dynamic output module	A1S42Y	16-, 32-, 48-, and 64-point 12/24 VDC dynamic output module	Number of set points (Outputs [ ])	0.10	0.008		
Blank cover	A1SG60	Keep unused slots from dust.	16 [empty]	—	—		
Dummy module	A1SG62	16-, 32-, 48-, and 64-input selectable module	Number of set points ([ ] inputs)	—	—		

* : Class 2 power supply specified by the UL/CSA Standard must be used.

Item	Model	Description		Number of Inputs/ Output	Current Consumption		Remarks	* Approved Standard
					DC5V(A)	DC12V(A)		
40-pin connector	A6CON1	Soldered joint type	Sink type	—	—	—		UL/CSA
	A6CON1E		Source type					
	A6CON2	Solderless attachment type	Sink type					
	A6CON2E		Source type					
	A6CON3	Pressed joint type	Sink type					
	A6CON3E		Source type					
Positioning module	A1SD70	Analog output, 1 axis		48 (first half: vacant 16 points, second half: special 32 points)	0.3	—		
	A1SD71-S2	Pulse output, 2 axes			0.8	—		
	A1SD71-S7	Pulse output, 2 axes (MPG can be used.)			0.8	—		
MELSECNET/ MINI-S3 data link module	A1SJ71PT32-S3	Master module for fiber-optic/ twisted-wire pair cable		32/45 (special 32 points/special 48 points)	0.35	—	The number of occupying points in I/O exclusive mode: 32, in extension mode: 48	
Analog I/O module	A1S63ADA	Analog input: 2 channels Analog output: 1 channel		32 (speical 32 points)	0.8	—		
Pulse catch module	A1SP60	Pulse input module with short ON time (Pulse : min. 0.5 msec) 16-point inputs		16 [16 outputs]	0.055	—		
Analog timer module	A1ST60	For changing timer set values(0.1 to 1.0 sec, 1 to 10 sec, 10 to 60 sec, 60 to 600 sec) by using volume adjustment knobs. Analog timer 8 points		16 [16 outputs]	0.055	—		
Interruption module	A1SI61	Interruption module for interruption program execution designation (Input for interruption : 16 points)		32 [Special 32-point]	0.057	—		
High-speed counter module	A1SD61	32-bit signed binary 50 KBPS, 1 channel		32 [Special 32-point]	0.35	—		
A-D converter module	A1S64AD	4 to 20 mA / 0 to 10 V Analog 4 channels		32 [Special 32-point]	0.4	—		
Temperature-digital converter module	A1S62RD3	For connecting a Pt100 (3-lead type) Temperature input: 2 channels		32 [Special 32-point]	0.54	—		
	A1S62RD4	For connecting a Pt100 (4-lead type) Temperature input: 2 channels		32 [Special 32-point]	0.44	—		
D-A converter module	A1S62DA	4 to 20 mA / 0 to 10 V Analog output: 2 channels		32 [Special 32-point]	0.8	—		
Computer link module	A1SJ71C24-R2	Computer link function RS-232C: 1 channel		32 [Special 32-point]	0.1	—		
	A1SJ71C24-PRF	Computer link and printer functions RS-232C: 1 channel		32 [Special 32-point]	0.1	—		
	A1SJ71C24-R4	Computer link and multidrop link functions RS-422/485: 1 channel		32 [Special 32-point]	0.1	—		

* : Class 2 power supply specified by the UL/CSA Standard must be used.

Item	Model	Description	Number of Inputs/ Output	Current Consumption		Remarks	* Approved Standard
				DC5V(A)	DC12V(A)		
MELSECNET (II) data link module	A1SJ71AP21	For master or local station of MELSECNET (II) optical data link	32 [Special 32-point]	0.5	—		UL/CSA
	A1SJ71AR21	For master or local station of MELSECNET (II) coaxial data link	32 [Special 32-point]	0.9	—		
MELSECNET /B data link module	A1SJ71AT21B	For master or local station of MELSECNET/B data link system	32 [Special 32-point]	0.66	—		
Main base unit	A1S32B	Up to two I/O modules can be loaded.	—	—	—	Equipped with two extension connectors : one is on the right; the other on the left side	
	A1S33B	Up to three I/O modules can be loaded.	—	—	—		
	A1S35B	Up to five I/O modules can be loaded.	—	—	—		
	A1S38B	Up to eight I/O modules can be loaded.	—	—	—		
Extension base unit	A1S52B(S1)	Up to two I/O modules can be loaded.	—	—	—	Power supply module cannot be loaded. (Power is supplied from the main base module.)	UL/CSA (except for S1 type)
	A1S55B(S1)	Up to five I/O modules can be loaded.	—	—	—		
	A1S58B(S1)	Up to eight I/O modules can be loaded.	—	—	—		
	A1S65B(S1)	Up to five I/O modules can be loaded.	—	—	—	Needs a power supply module.	
	A1S68B(S1)	Up to eight I/O modules can be loaded.	—	—	—		
Extension cable	A1SC01B	55 mm (2.17 inch) long flat cable	—	—	—	For extension on the right side	UL/CSA
	A1SC03B	330 mm (11.8 inch) long	—	—	—	Extension base unit connection cable	
	A1SC07B	700 mm (27.6 inch) long	—	—	—		
	A1SC12B	1200 mm (47.24 inch) long	—	—	—		UL/CSA
	A1SC30B	3000 mm (118.11 inch) long	—	—	—		
	A1SC60B	6000 mm (236.22 inch) long	—	—	—		
	A1SC05NB	450 mm (17.72 inch) long	—	—	—	A[ ]N, A[ ]A extension base cable	UL/CSA
	A1SC07NB	700 mm (27.6 inch) long					
Memory cassette EPROM	A2SMCA-14KP	14K steps equipped with ROM (directly)	—	—	—	Needs a memory write adapter.	UL/CSA
Memory cassette EEPROM	A2SMCA-14KE	14K steps equipped with 28K EROM (directly)	—	—	—	Direct write/read from peripheral devices can be done.	
Memory write adapter	A2SWA-28P	Used for memory cassette connector/EPROM 28-pin.	—	—	—	Used to partition ROM in EPROM memory cassette.	
Battery	A6BAT	IC-RAM memory backup	—	—	—		

* : Class 2 power supply specified by the UL/CSA Standard must be used.

Item	Model	Description	Applicable Model
Connector/ terminal block conversion module	A6TBXY36	For sink type input module and sink type output module (standard type)	A1SX41(S2), A1SX42(S2), A1SY41, A1SY42, A1SH42
	A6TBXY54	For sink type input module and sink type output module (2-wire type)	AX42(S1), AY42(S1/S3/S4), AH42
	A6TBX70	For sink type input module (3-wire type)	A1SX41(S2), A1SX42(S2), A1SH42, AX42(S1), AH42
	A6TBX36-E	For source type input module (standard type)	A1SX81(S2), AX82
	A6TBY36-E	For source type output module (standard type)	A1SY81, AY82EP
	A6TBX54-E	For source type input module (2-wire type)	A1SX81(S2), AX82
	A6TBY54-E	For source type output module (2-wire type)	A1SY81, AY82EP
	A6TBX70-E	For source type input module (3-wire type)	A1S81(S2), AX82
Cable for connector/ terminal block conversion module	AC05TB	0.5 m (1.64 ft) for source module	A6TBXY36 A6TBXY54 A6TBX70
	AC10TB	1 m (3.28 ft) for source module	
	AC20TB	2 m (6.56 ft) for source moduel	
	AC30TB	3 m (9.84 ft) for source module	
	AC50TB	5 m (16.4 ft) for source module	
	AC05TB-E	0.5 m (1.64 ft) for source module	A6TBX36-E
	AC10TB-E	1 m (3.28 ft) for source module	A6TBY36-E
	AC20TB-E	2 m (6.56 ft) for source module	A6TBX54-E
	AC30TB-E	3 m (9.84 ft) for source module	A6TBY54-E
	AC50TB-E	5 m (16.4 ft) for source module	A6TBX70-E

REMARK

I/O cables with connectors for I/O modules of 40-pin connector specifications (A1SX41, A1SX42, A1SY41, A1SY42, etc.) or 37-pin D-sub connector specificaions (A1SX81, A1SY81) are available.
Consult the nearest Mitsubishi representative for the I/O cables with connectors.

(1) A[ ]NA[ ]A extension base unit

The following table shows the modules that can be loaded to the A[ ]NA[ ]A extension base units: A65B; A68B; A55B; or A58B.

For details on the specifications of each module see the appropriate manual of the module.

POINT

(1) All A[ ]NA[ ]A "building block type I/O modules" are applicable to the A2ASCPU.

Item	Model
Single-axis positioning module	AD70, AD70D
Positioning module	AD71, AD71S1, AD72
Position detection module	A61LS, A62LS
High speed counter module	AD61, AD61S1
A-D converter module	A68AD, A68ADS2, A616AD, A60MX A60MXR, A68ADN
Temperature digital converter module	A616TD, A60MXT
D-A converter module	A62DA, A62DAS1, A616DAI, A616DAV, A68DAV, A68DAI
A-D/D-A converter module	A84AD
CRT control/LCD control module	AD57, AD57S1, AD58
Graphic controller module	AD57G, AD57GS3
Memory card, Centronics interface module	AD59, AD59S1
Voice output module	A11VC
Computer link module	AJ71C24(S3/S6/S8), AJ71UC24
Intelligent interface module	AD51E, AD51ES3, AD51H(S3)
Terminal interface module	AJ71C21, AJ71C21S1
MELSECNET/MINI (S3) data link module	AJ71PT32, AJ71PT32-S3
Data link module	AJ71AP21, AJ71AR21, AJ71AT21B
SUMINET interface module	AJ71P41
Ethernet interface module	AJ71E71
Multidrop data link module	AJ71C22
Interrupt module	AI61
Power supply module	A61P, A62P, A63P, A65P, A66P, A68P
Extension base module	A62B, A65B, A68B, A52B, A55B, A58B

(2) Peripheral devices

Item	Module	Remarks	
Plasma handy graphic programmer	A6PHP-SET	• A6PHP • SW4GP-GPPAEE: A-series GPP function system disk (Compatible with A2ACPU(S1) or equivalent only) • SW0-GPPU: User disk (2DD) • AC30R4: RS-422 cable (3 m (9.84 ft) length)	
Intelligent GPP	A6GPP-SET	• A6GPP • SW4GP-GPPAEE: A-series GPP function system disk (Compatible with A2ACPU(S1) or equivalent only.) • SW0-GPPU: User disk (2DD) • AC30R4: RS-422 cable (3 m (9.84 ft) length)	
Handy graphic programmer	A6HGP-SET	• A6HGP (Compatible with A3HCPU or equivalent only.) • SW3-HGPA: A-series GPP function system disk • SW1-HGPK: K-series GPP function system disk • SW0-GPPU: User disk (2DD) • AC30R4: RS-422 cable (3 m (9.84 ft) length)	
Composite video cable	AC10MD	• Connects between A6GPP and monitor display. (1 m (3.28 ft) length)	
RS-422 cable	AC30R4	3 m (9.84 ft) length	Connects between CPU and A6GPP/A6PHP.
	AC300R4	30 m (98.4 ft) length	
User disk	SW0-GPPU	2DD	Used for storing user program (3.5 inch, formatted)
	SW0S-USER	2HD	
Cleaning disk	SW0-FDC	Applicable to A6GPP/A6PHP	Used for cleaning disk drive.
Programming unit	A8PUE	• Compatible with A2ACPU(S1) or equivalent only.	
	A7PU, A7PUS	• Compatible with A3HCPU or equivalent only.	
RS-422 cable	AC20R4-A8PU	Connects between CPU and A8PUE/A7PUS. 2m/3m (6.56 ft/9.84 ft) length	
	AC30R4-PUS		
P-ROM writer module	A6WU	• Used for writing a program in CPU/A6PHP to ROM, or for reading a CPU program from ROM. (Compatible with A3HCPU or equivalent.) • Connected to CPU/A6PHP using an AC30R4/AC03WU cable.	
RS-422 cable	AC30R4, AC300R4	Connects between CPU and A6WU. 3 m/30 m (9.84 ft/98.4 ft) length	
	AC03WU	Connects between CPU and A6WU. 0.3 m (0.99 ft) length	

2.3 General Description of System Configuration

This section gives a brief general description of independent, data link, computer and combined link systems.

The A2ASCPU may be used in the following system configurations.

(1) Independent system

System which consists of only the main base unit or of the main base unit and extension base unit(s) which are connected by the extension cable(s).

(2) Network system

System which allows data communication between a network of programmable controllers and I/O modules at remote locations.

(3) Computer link system

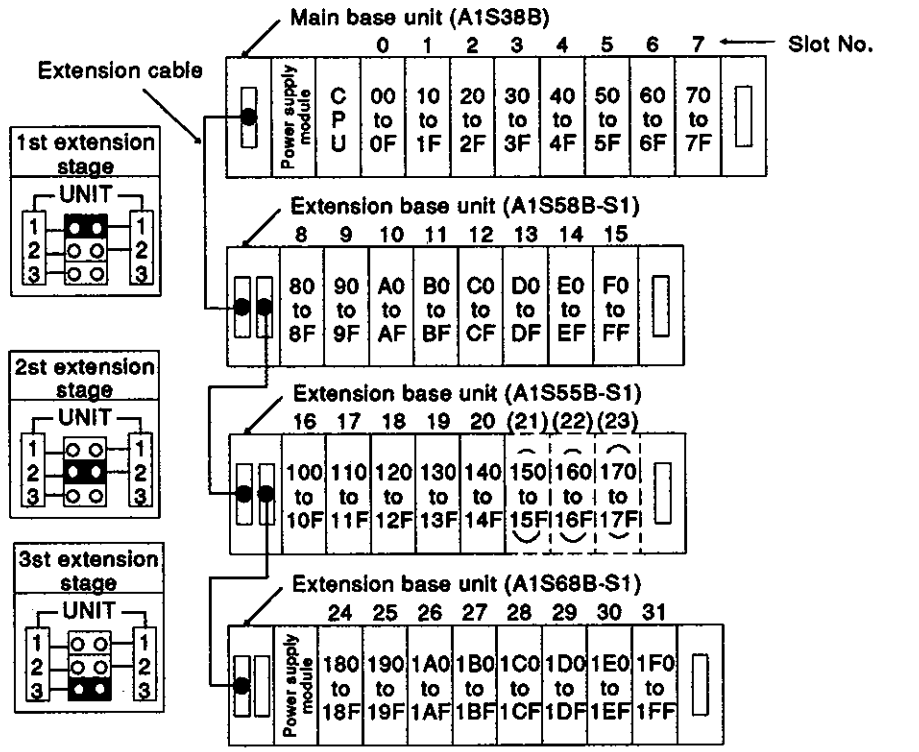
System to make data transfer between the A2ASCPU and computer (such as a personal computer) using the computer link module AJ71UC24.

(4) Combined system

System which combines the network system and computer link system.

The system configuration, number of I/O points, I/O assignment, etc. for an independent system are described on the next page.

(5) The following shows the system configuration, the number of input/output points, and I/O number allocation when the A2ASCPU is used as an independent system.

System configuration	 * The above figure shows the configuration when 16-input/output modules are loaded to each slot.
Maximum Number of Extension Stages	Three Extension Stages
Maximum number of input/output points	A2ASCPU: 512 points, A2ASCPU-S1: 1024 points
Main base units	A1S32B, A1S33B, A1S35B, A1S38B
Extension base units	A1S52B(S1), A1S55B(S1), A1S58B(S1), A1S65B(S1), A1S68B(S1), A52B, A55B, A58B, A62B, A65B, A68B
Extension cables	A1SC01B, A1SC03B, A1SC07B, A1SC12B, A1SC30B, A1SC60B, AC06B, AC12B, AC30B, A1SC05NB, A1SC07NB
Notes	(1) Only the 1st extension stage can be used when extension base units of other types than the A1S S1 are equipped. (The S1 type and other types must not be used together.) (2) To use the A1S S1 type extension base unit with an A[ ]N or A[ ]A type, the latter must be equipped with the last extension stage. (The A[ ]N or A[ ]A extension base unit cannot be connected to the A1S S1 type.) (3) When an A1S52B (S1), A1S55B (S1), A1S58B (S1), A52B, A55B, or A58B is used, a voltage of 5 VDC is supplied from the power supply module. See Section 7.1.3, and consider the application. (4) The extension cable should be used for distances of up to 6m (19.68 ft).
I/O number allocation	(1) Allocate I/O numbers to the extension base units in order of extension stage number, not in extension cable connection order. (2) I/O numbers are allocated on the assumption that both the main base unit and the extension base units have eight slots. Sixteen input/output points will be allocated to each slot indicated by dotted lines in the above system configuration figure. (3) Allocate 16 input/output points to an empty slot. (4) If the setting of extension stages has been omitted, make allocation on the assumption that each slot is occupied with 16 input/output points as to the eight slots of all the omitted stages. (5) Items (2) to (4) can be changed by making "I/O allocation". For details, see the ACPU Programming Manual (Fundamentals).

2.4 Cautions on System Configurations

Described below are the modules, peripheral devices and software packages compatible with the A2ASCPU.

2.4.1 Modules and peripheral devices

(1) I/O module

All A[ ]N and A[ ]A building block type I/O modules are applicable to the A2ASCPU by loading them to the A5[ ]B and A6[ ]B extension base units.

(2) Special function module

(a) An A[ ]N or A[ ] A special function module can be used by loading it to the A5[ ]B or A6[ ]B extension base unit.

(b) Among the special function modules, the following types must not be loaded in excess of the quantities specified below:

AD51(S3)*1 AD51H(S3)*2 AD51FD*2 AD57G(S3)*2 AJ71C22*1 AJ71C24(S3/S6/S8)*1,*2 AJ71C24*3 AJ71UC24*1, *2 AJ71P41*1 AJ71E71*2	Up to 6 in total
A1SJ71C24-R2(PRF/R4)*2	
AI61(S1)*3	Only 1
A1SI61*3	
AJ71AP21*2 AJ71AP21*2 AJ71AT21B*2	
A1SJ71AT21B*2	

*1: Accessible within the device range of the A3HCPU only. (The AJ71C24-S8 is accessible within the device range of the A2ASCPU.)
*2: Accessible within the device range of the A2ACPU only.
*3: Accessible within any device range.

REMARK

The special function modules below cannot be used with the A2ASCPU:

- AJ71C23
- AD57-S2
- AJ71C24 (module manufactured before February 1987)
- AD51 (module manufactured before March 1987)
  Check the date of manufacture with the label.

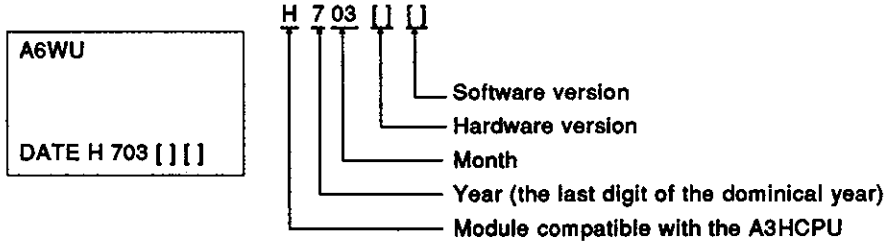
(3) Peripheral device

(a) Use an A6WU P-ROM writer whose software version is "E" or subsequent to it.

(b) The A6PU cannot be used.

(c) The A6WU and the A7PU are usable within the device range of the A3HCPU only.

Description of the label <EX.> Module manufactured in March 1987



(4) Memory cassette

Partitioning the ROM in the A2SMCA-14KP EPROM memory cassette using an A6GPP/A6WU/ROM writer requires an A2SWA-28P memory write adaptor (option). (Existing A6WA-28P memory write adaptor cannot work.)

Cautions on writing to A2SMCA-14KE EEPROM memory cassette

1) When an operation is done using the EEPROM, writing at RUN gives the peripheral devices the message "PROGRAM BEING TRANSFERRED", and stops the sequence program for about two seconds after the transfer, completing writing at RUN.
If the two-second suspension of the sequence program influences the control devices, do not perform writing at RUN, but stop the CPU to write.

2) To do writing to the EEPROM using an existing system FD, turn OFF the EEPROM memory protect switch.
If the switch is ON, a memory protect error occurs. Writing at RUN to the EEPROM also becomes invalid.

2.4.2 Software packages

(1) A series system FD

Prior to using an existing system FD, set the PC type displayed on the initial data setting screen to either of the following, and prepare a sequence program.

- Setting to A3H (A3H-associated system FD) ..... Available within the device range of the A3HCPU only.
- Setting to A2A (AnA-associated system FD) ..... Available within the device range of the A2A only.

The following software packages cannot be used because the PC is unavailable in the A3HCPU and A2ACPU types:

- SW0-GPPA, SW1-GPPA, SW2-GPPA
- SW2-HGPA

See APPENDIX 1 for applicable combinations of software packages and peripheral devices.

(2) Utility package

(a) The following utility packages for the A6GPP/A6PHP cannot be used.

- SW[ ]-AD57P
- SW[ ]-UTLP-FN0
- SW[ ]-UTLP-FN1
- SW[ ]-UTLP-PID

Functions same as those available with the utility packages mentioned to the left can be executed by using dedicated instructions.
Refer to the AnACPU Programming Manual (Dedicated Instructions) for details.

REMARK

The necessary character generator and canvas when using the AD57(S1) and AD58 units are created on peripheral devices by using the SW[ ]-AD57P.

(b) Device ranges are partially restricted when using the following utility packages for PC/AT.

- SW0IX-SAP2E
- SW0IX-AD57GPE
- SW1IX-AD57GPE
- SW0IX-AD51HPE
- MELSEC-MEDOC

Can be used in the device range equivalent to that of A2ACPU(S1).

POINT

Utility packages used to make access to the A2ASCPU by designating the devices can be used in the device range equivalent to that of A2ACPU(S1) or A3HCPU.

3. GENERAL SPECIFICATIONS

Table 3.1 shows the common specifications of various modules used.

Table 3.1 General Specifications

Item	Specifications				
Operating ambient temperature	0 to 55°C				
Storage ambient temperature	–20 to 75°C				
Operating ambient humidity	10 to 90%RH, non-condensing				
Storage ambient humidity	10 to 90%RH, non-condensing				
Vibration resistance	Conforms to * JIS C 0911	Frequency	Acceleration	Amplitude	Sweep Count
		10 to 55Hz	———	0.075mm (0.003 inch)	10 times *(1 octave /minute)
		55 to 150Hz	9.8 m/s^2 (1g)	———	
Shock resistance	Conforms to JIS C 0912 (98 m/s^2 (10g) × 3 times in 3 directions)				
Noise durability	By noise simulator of 1500Vpp noise voltage, 1 μs noise width and 25 to 60Hz noise frequency				
Dielectric withstand voltage	1500 VAC for 1 minute across AC external terminals and ground 500 VAC for 1 minute across DC external terminals and ground				
Insulation resistance	5MΩ or larger by 500 VDC insulation resistance tester across AC external terminals and ground				
Grounding	Class 3 grounding; Ground to the panel if proper grounding is not available.				
Operating ambience	Free of corrosive gases and oil mist. Dust should be minimal.				
Cooling method	Self-cooling				

REMARK

One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10Hz to 20Hz, from 20Hz to 40Hz, from 40Hz to 20Hz, and 20Hz to 10Hz are referred to as one octave.

Note: * JIS: Japanese Industrial Standard

4. CPU MODULE

4.1 CPU Module Performance Specifications

This section explains the performance specifications and devices of the A2ASCPU.

Table 4.1 Performance Specifications

Item			Performance		Remarks
			A2ASCPU	A2ASCPU-S1	
Control system			Stored program, repeated operation		
I/O control method			Refresh method		Instructions to enable partial direct I/O are available.
Programming language			Language dedicated to sequence control		
			Combined use of relay symbol type, logic symbolic language and MELSAP-II(SFC)		
Processing speed (Sequence instruction) (μ sec/step)			0.2		
Instruction (types)	Sequence instruction		22		
	Basic, application instruction		239		
	Dedicated instruction		200		
Constant scan (program start at specified intervals)			Can be set between 10 msec and 190 msec in 10 msec increments		Set in special register D9020.
Memory capacity			64 kbytes (built-in RAM)	256 kbytes (built-in RAM)	A2SMCA-14KP/14KE (64 kbytes) can be installed.
Program capacity	Main sequence program		Max. 14K steps		Set in parameters.
	Sub-sequence program		Absent		
I/O device points			8192 points (X/Y0 to 1FFF)		The number of points usable in the program
I/O points			512 points (X/Y0 to 1FF)	1024 points (X/Y0 to 3FF)	The number of points which can be used for accessibility to I/O modules
Device points	Internal relay (M)		7144 points (M0 to M999, M2048 to M8191)	Total of 8192 points shared by M, L, and S	Range of each device can be changed in parameters.
	Latch relay (L)		1048 points (L1000 to L2047)		
	Step relay (S)		0 point (None in the initial state)		
	Link relay (B)		4096 points (B0 to BFFF)		
	Timer (T)		2048 points (defaults to 256 points) • 100 msec timer (T0 to T199) ..... Setting range 0.1 to 3276.7 sec • 10 msec timer (T200 to T255) ..... Setting range 0.01 to 327.67 sec • 100 msec retentive timer ..... Setting range 0.1 to 3276.7 sec (None in the initial state) • Extension timer ..... Set range with word devices (T256 to T2047) (D, W, R)		Set number of points used and range in parameters. (Refer to Section 4.4.1.)
	Counter (C)		1024 points (defaults to 256 points) • Normal counter (C0 to C255) ..... Count range 1 to 32767 times • Interrupt counter ..... Can be set within the range of C224 to C255 depending on the setting (None in the initial state) • Extension counter ..... Set range with word devices (C256 to C1023) (D, W, R)		Set number of points used and range in parameters. (Refer to Section 4.4.1.)
	Data register (D)		6144 points (D0 to D6143)		
	Link register (W)		4096 points (W0 to WFFF)		
	Annunciator (F)		2048 points (F0 to F2047)		Device for fault detection
	File register (R)		8192 (R0 to R8191)		Set number of points in parameters.

Table 4.1 Performance Specifications (Continued)

Item		Performance		Remarks
		A2ASCPU	A2ASCPU-S1	
Device points	Accumulator (A)	2 points (A0, A1)		
	Index register (V, Z)	14 points (V, V1 to V6, Z, Z1 to Z6)		
	Pointer (P)	256 points (P0 to P255)		
	Interrupt pointer (I)	32 points (I0 to I31)		
	Special relay (M)	256 points (M9000 to M9255)		
	Special register (D)	256 points (D9000 to D9255)		
Comment		Max. 4032 points (Set in units of 64 points)		Set in parameters.
Extension comment		Max. 3968 points (Set in units of 64 points)		
Output mode switching at STOP → RUN		Selection of re-output of operation state before STOP (default)/output after operation execution		Set in parameters.
Self-diagnostic functions		Watchdog timer (watchdog timer 200 msec fixed) Memory error detection, CPU error detection, I/O error detection, battery error detection, etc.		Refer to Section 4.3.1 for details.
Operation mode at error occurrence		Stop or continue selectable		Set in parameters. (Refer to Section 4.4.1.)
Starting method at RUN		Initial start (Automatic restart when "RUN" switch is moved to ON position at power-on, at power restoration after power failure)		
Latch (power failure compensation) range		Defaults to L1000 to L2047 (Latch range can be set for L, B, T, C, D and W relays.)		Set range in parameters.
Remote RUN/PAUSE contact		One RUN contact and one PAUSE contact can be set within the range from X0 to X1FF (A2AS) or X3FF (A2AS-S1)		Set in parameters.
Print title entry		Available (128 characters)		Set in parameters.
Entry code		Available		Set in parameters.
I/O allocation		Number of occupied I/O points and unit model can be entered.		
Step RUN		Can execute or stop sequence program operation.		Refer to Section 4.3.
Interrupt processing		Interrupt program can be run in response to a signal from an interrupt unit or by a constant-cycle interrupt signal.		
Data link		MELSECNET(II)		
Allowable momentary power failure time		Depends on used power supply module		Refer to Section 6.1.
5 VDC internal power consumption (A)		0.32		
Weight kg (lb)		0.41 (0.9)		
External dimensions mm (in)		130 x 54.5 x 93.6 (5.12 x 2.15 x 3.69)		

CAUTION

When the existing system software package and peripheral devices are used, the applicable device range is limited. Refer to Section 1.3 for details.

4.2 Device List

The range of use of A2ASCPU devices which can be specified using an AnA compatible system FD is shown in Table 4.2.
Note the items marked "*" in the table, since the range of use is restricted when using a conventional system FD and peripheral devices.

Table 4.2 Device List

Device			Application Range (Number of points)		Explanation
			A2ASCPU	A2ASCPU-S1	
*	X	Input	X, Y 0 to 1FF (512 points)	X, Y 0 to 3FF (1024 points)	rovides PC command and data from external devices, e.g., pushbutton, select switch, limit switch, and digital switch.
*	Y	Output			Provides program control result to external devices, e.g., solenoid, magnetic switch, signal light, and digital display.
	M	Special relay	M9000 to 9255 (256 points)		Predefined auxiliary relay for special purpose and for use in the PC.
*		Internal relay	M/L/S 0 to 8191 (8192 points) Number of Ms + Ls + Ss = 8192 points		Auxiliary relay in the PC which cannot be output directly.
*	L	Latch relay			Auxiliary relay in the PC which cannot be output directly. Backed up during power failure.
*	S	Step relay			Used in the same manner as an internal relay (M), e.g. as a relay indicating the stage number of a step-by-step process operation program.
*	B	Link relay	B0 to BFFF (4096 points)		Internal relay for data link which cannot be output. May be used as an internal relay if not set for link initial data.
*	F	Annunciator	F0 to F2047 (2048 points)		Used to detect a fault. When switched on during RUN by a fault detection program, stores a corresponding number in special register D.
*	T	100 msec timer	T0 to T2047 (2048 points) (After T256, set value storage registers required)		Up timers available in 100 msec, 10 msec and 100 msec retentive types.
		10 msec timer			
		100 msec retentive timer			
*	C	Counter	C0 to C1023 (1024 points) (Interrupt counter C224 to C255 fixed. After C256, set value storage registers required)		Up counters available in normal and interrupt types.
		Interrupt counter			

Table 4.2 Device List (Continued)

Device			Application Range (Number of points)		Explanation
			A2ASCPU	A2ASCPU-S1	
*	D	Data register	D0 to D6143 (6144 points)		Memory for storing PC data.
		Special register	D9000 to D9255 (256 points)		Predefined data memory for special purpose.
*	W	Link register	W0 to WFFF (4096 points)		Data register for use with data link.
	R	File register	R0 to R8191 (8192 points)		Extends data register using user memory area.
	A	Accumulator	A0, A1 (2 points)		Data register for storing the operation results of basic and application instructions.
*	Z V	Index register	V, V_1 to V_6, Z, Z_1 to Z_6 (14 points)		Used to modify devices (X, Y, M, L, B, F, T, C, D, W, R, K, H, P).
	N	Nesting	N0 to N7 (8 levels)		Indicates the nesting of master controls.
	P	Pointer	P0 to P255 (256 points)		Indicates the destination of the branch instruction (CJ, SCJ, CALL, JMP).
	I	Pointer for interruption	I0 to I31 (32 points)		Indicates the destination of an interrupt program corresponding to the interrupt factor which has occurred.
	K	Decimal constant	K-32768 to 32767 (16-bit instruction) K-2147483648 to 2147483647 (32-bit instruction)		Used to specify the timer/counter set value, pointer number, interrupt pointer number, the number of bit device digits, and basic and application instruction values.
	H	Hexadecimal constant	H0 to FFFF (16-bit instruction) Ho to FFFFFFFF (32-bit instruction)		Used to specify the basic and application instruction values.

4.3 Function List

(1) Refer to the following manual for the details of functions (operations, program examples, etc.)
• ACPU Programming Manual (Fundamentals)

(2) Refer to the operating manual for the specific peripheral device for the operation of functions.

(3) Functions for which reference sections are given in the table below are explained in this manual.

Table 4.3 Function List

Function (Application)	Description	Settings and operations
Constant scan [•Program execution at fixed intervals. •Simple positioning]	• The sequence program is executed while maintaining a constant scan time. • The range for the constant scan time setting is from 10 msec to 190 msec in units of 10 msec.	• The set value is written to special data register D9020.
Latch (power failure backup) [Continued control by retaining data at power failure]	• Retains data of latched devices when momentary power failure occurs 20 msec or longer, CPU is reset, or power is turned OFF. • L, B, T, C, D and W can be latched. • The data in the latch range is stored in the CPU module and is backed up by the battery in the memory cassette.	• Latch devices and latch ranges are set by using the parameter setting on peripheral devices.
MELSECNET/MINI-S3 automatic refresh [Simplification of sequence program]	• I/O automatic refresh communications with the send/receive data area for partial refresh of up to 8 AJ71PT32-S3 modules are executed. • Automatic refresh is executed in batch after END processing. • The FROM/TO instructions for input/output used with the sequence program are not necessary. Allocated I/O devices can be used directly for programming.	• Use automatic refresh parameter setting of peripheral devices. (Refer to Section 4.4.5.)
Remote RUN/STOP [PC RUN/STOP is controlled by an external device.]	• When PC CPU is in the RUN state (key switch at RUN), PC RUN/STOP is controlled by an external device (external input, peripheral device, computer).	• To use an external input (X), set parameter by a peripheral device. • To use a peripheral device, use the PC test mode. • To use a computer through a computer link module, use a special command.
PAUSE [•Stops CPU operation while retaining the output (Y). •PC RUN/PAUSE control is externally executed.]	• PC CPU operation is stopped while retaining the ON/OFF status of all outputs (Y). [When operation is stopped by STOP, all outputs (Y) are turned OFF.] • When PC CPU is in the RUN state (key switch at RUN), PC RUN/PAUSE is controlled by an external device (external input, peripheral device, computer).	• To use a peripheral device, use the PC test mode. • To use an external input (X), set parameter by a peripheral device, and turn M9040 ON by using the sequence program.
Status latch [Used to check device status and fault factors when debugging or when a fault factor is established.]	• When status latch condition is established, status of devices set for status latch is stored to the extension file register in the status latch area in the memory cassette. (Stored data can be cleared by latch clear operation.) Condition establishment can be set for the • SLT instruction execution by sequence program or for the matching of set condition with device value.	• Set the status latch devices and the extension file registers to store latched data by using a peripheral device. Monitor status latch data by • a peripheral device.

Table 4.3 Function List (continued)

Function (Application)	Description	Settings and operations
Sampling trace [Used to check function of devices tracing the time when debugging or when operation is fauity.]	• Devices set for sampling trace are sampled by scan or set time intervals for set number of times, and the result is stored to the extension file registers for sampling trace in the memory cassette. (Stored data can be cleared by latch clear operation.) • Sampling trace is executed by executing a STRA instruction by the sequence program.	• Set the sampling trace devices, trace points, number of times and the extension file registers to store traced data by using a peripheral device. • Monitor sampling trace results by a peripheral device.
Step run [Used to check program execution condition and operation when debugging.]	• Sequence program operation is executed under the following (1) to (5) conditions and then stopped. (1) Execution by instruction (2) Execution by circuit block (3) Execution by step interval and loop count (4) Execution by loop count and break point (5) Execution when device value is matched	• Select step run condition by a peripheral device, and set for execution.
Clock [Program management by clock data/external display of clock data]	• Clock built in the CPU module is operated. • Clock data: Year, month, day, hour, minute, second, day of the week • Clock data is read and stored to D9025 to D9028 by a clock device after sequence program END processing when a clock data read request M9028 is ON. • Clock device is backed up by the battery in the memory cassette.	• Set data to D9025 to D9028 by a peripheral device, and turn ON M9025 to write clock data to the clock device. • Use the sequence program to write to the clock device (dedicated instructions can be used).
LED display priority [Changes display priority/ display cancel]	• Display priority is changed/canceled for errors except the errors which stop operation and default display items of the LED display.	• Use the sequence program to write priority/display cancel data to D9038 and D9039.
Self diagnosis [CPU operation fault detection, preventive maintenance]	• Stops CPU operation when an error included in the self diagnosis items occurs when the CPU is powered ON or running, and displays error message for malfunction prevention. •Stores error code corresponding to the self diagnosis items.	• Parameter setting by peripheral device can control operation to stop or continue. Read error codes by peripheral device and perform troubleshooting. (Refer to Section 4.3.1.)

4.3.1 Self-Diagnosis

The self-diagnosis function permits the CPU to detect its own errors.

(1) Self- diagnosis is carried out when the PC power supply is turned on and when an error occurs while the PC is in the RUN state. If the CPU detects an error, it displays the error and stops operation to prevent faulty PC operation.

(2) The A2ASCPU stores the last occurring error in the error code area (special register D9008). Then it stores detailed error code in special register D9091.

(3) Even when the power has been turned OFF, the most recent error information of up to 16 error occurrences is stored due to battery backup. With an A2ASCPU compatible system FD, error data on up to 16 error occurrences can be confimed with a peripheral device. Use the "latch clear" function of the CPU module to reset (all clear) stored error infomation. The content of error information is shown below.

(a) Occurrence time : Year, month, date, hour, minute, second (clock data)

(b) Error code : Content of special register D9008

(c) Detailed error code : Content of special register D9091

(d) Error step and faulty module loading address : Content of special registers D9010, D9000, and D9002

(4) The PC may operate in one of two modes when an error is detected by the self-diagnosis function. In the stop mode, PC operation is stopped when the error is detected; in the continue mode, PC operation is continued. In the continue mode, however, parameters can be set to cause opetaion to stop if specified errors occur.

(a) Operation stops and all outputs (Y) turn off immediately the self-diagnosis function detedts an error whch stops PC operation.

(b) If the self-diagnosis function detects an error at which PC operation continues, the part of the program where the error was detected is skipped and the rest of the program esecuted.

If an I/O module verify error is detected, operation is continued with the I/O addresses at the time the error occurred. Any detected error is stored in a special relay (M) or special register (D).

In the continue mode, in particular, the program should read the details of the error and take appropriate action to prevent fanlty PC and machine operation.

Explanations of the errors detected by the self-diagnosis function are listed in Table 4.4.

REMARKS

(1) The display priority of LED display messages can be changed when the CPU is in operation mode. (The error code is stored in special register.)
(2) The fuse blow, I/O verify and battery check are not checked when M9084 is on. (The error code is not stored in special register.)

Table 4.4 Self-Diagnosis List

Diagnosis		Diagnosis Timing	CPU Status	"RUN" LED Status	LED Display Message	Error code (D9008)
Memory error	Instruction code check	When the corresponding instruction is executed	Stop	Flicker	INSTRCT. CODE ERR.	10
	Parameter setting check	When power is switched on or reset performed When switched from STOP/PAUSE to RUN/ STEP-RUN			PARAMETER ERROR	11
	No END instruction	When M9056 or M9057 is switched on When switched from STOP/PAUSE to RUN/STEP-RUN			MISSING END INS.	12
	Instruction execution disable	When CJ, SCJ, JMP, CALL(P), FOR and NEXT instruction is executed When switched from STOP/PAUSE to RUN/STEP-RUN			CAN'T EXECUTE (P)	13
	Format (CHK instruction) check	When switched from STOP/PAUSE to RUN/STEP-RUN			CHK FORMAT ERR.	14
	Instruction execution disable	When interrupt occurs When switched from STOP/PAUSE to RUN/STEP-RUN			CAN'T EXECUTE (I)	15
CPU error	RAM check	When power is switched on or reset performed When M9084 is switched on during STOP	Stop	Flicker	RAM ERROR	20
	Operation circuit check	When power is switched on or reset performed			OPE. CIRCUIT ERR.	21
	Watchdog error check	When END instruction is executed			WDT ERROR	22
	END instruction unexecution	When END instruction is executed			END NOT ERROR	24
	Main CPU check	At any time			MAIN CPU DOWN	26
I/O error	I/O module verify *1: default: STOP	When END instruction is executed (Not checked when M9084 or M9094 is on)	Stop / Run	Flicker / On	UNIT VERIFY ERR.	31
	Fuse blow *1: default: RUN	When END instruction is executed (Not checked when M9084 or M 9094 is on)			FUSE BREAK OFF.	32

*1: Can be changed by parameter setting on peripheral devices.

Table 4.4 Self-Diagnosis List (Continued)

Diagnosis		Diagnosis Timing	CPU Status	"RUN" LED Status	LED Display Message	Error code (D9008)
Special function module error	Control bus check	When FROM, TO instruction is executed	Stop	Flicker	CONTROL-BUS ERR.	40
	Special function unit error	When FROM, TO instruction is executed			SP. UNIT DOWN	41
	Link module error	When power is switched on or reset performed When switched from STOP/PAUSE to RUN/STEP-RUN			LINK UNIT ERROR	42
	I/O interruption error	When interrupt occurs			I/O INT. ERROR	43
	Special function module assignment	When power is switched on or reset performed When switched from STOP/PAUSE to RUN/STEP-RUN			SP. UNIT LAY. ERR.	44
	Special function module error *1: default: STOP	When FROM, TO instruction is executed	Stop / Run	Flicker / On	SP. UNIT ERR.	46
	Link parameter error	When power is switched on or reset performed When switched from STOP/PAUSE to RUN/STEP-RUN	Run	On	LINK PARA. ERROR	47
Battery error	Battery low	At any time (Not checked When M9084 is on)	Run	On	BATTERY ERROR	70
Operation check error *1: default: RUN		When the corresponding instruction is executed	Stop / RUN	Flicker / ON	OPERATION ERROR *2 "<CHK> ERROR[ ][ ][ ]"	50

*1: Can be changed by parameter setting on peripheral devices.

*2: An error only occurs when a CHK instruction is indicated with a 3-digit code.

4.4 Parameter Setting Range

Parameter setting ranges, user memory allocation contents, I/O device allocation method and automatic refresh of MELSECNET/MINI-S3 are explained in this section.

4.4.1 Parameter setting range list

Parameter setting involves specifying various PC functions and device ranges as well as allocating the user memory in the memory cassette.

The set data is stored in the parameter memory area (the first 3 Kbytes of the user memory area).

As given in the table below, default values can be used as they are set with parameter data. Setting ranges shown here can be changed by the peripheral device according to their purpose.

Table 4.5 Parameter Setting Range List

Setting / Item	Default Value	Type		Remarks (Refer to Appendix 1.) [When existing software package is used.]
		A2ASCPU	A2ASCPU-S1	
Main sequence program capacity	6K steps	1 to 14K steps (1K step = in units of 2 Kbytes)		• Usable with PC type A2A or A3H
File register	——	0 to 8K points (1K point = in units of 2 Kbytes)		• Usable with PC type A2A or A3H
Extension file register	——	1 block = 16 Kbytes (Block setting for block Nos. 1 to 8 and 10 to vacant memory area) [Automatically set to vacant memory area by file register setting.]		• Usable with PC type A2A Unusable with PC type A3H
Comment capacity	——	0 to 4032 points (in units of 64 points = in units of 1 Kbyte) [1 Kbyte memory area is added by setting a comment capacity.]		• Usable with PC type A2A or A3H
Extension comment capacity	——	0 to 3968 points (in units of 64 points = in units of 1 Kbyte)		• Usable with PC type A2A Unusable with PC type A3H
Status latch	——	Parameter setting is not provided.		• Usable with PC type A2A in the A2A's device range. • Set memory capacity with PC type A3H in the A3H's device range. (Refer to ACPU Programming Manual.)
Sampling trace	——	(Set the device and the resultant destination extension file register by the status latch and sampling trace modes. Refer to ACPU Programming Manual (Fundamentals).)		

Table 4.5 Parameter Setting Range List (Continued)

Item \ Setting		Default Value	Type		Remarks (Refer to Appendix 1) [When existing software package is used.]
			A2ASCPU	A2ASCPU-S1	
Setting of latch (power failure compensation) range	Link relay (B)	• Only for L1000 to L2047 • Absent for others.	B0 to BFFF (in units of 1 point)		• Usable with PC type A2A in the A2A's device range • Usable with PC type A3H in the A3H's device range
	Timer (T)		T0 to T255 (in units of 1 point) T256 to T2047 (in units of 1 point)		
	Counter (C)		C0 to C255 (in units of 1 point) C256 to C1023 (in units of 1 point)		
	Data register (D)		D0 to D6143 (in units of 1 point)		
	Link register (W)		W0 to WFFF (in units of 1 point)		
Setting of internal relay (M), latch relay (L), step relay (S)		M0 to M999 M2048 to M8191 L1000 to L2047 Absent for S	M/L/S 0 to 8191 (M, L, S are serial numbers)		• Usable with PC type A2A • Usable with PC type A3H in the A3H's device range
Setting of timer	T0 to T255	100 ms: T0 to T199 10 ms: T200 to T255	• 256 points of 100 ms, 10 ms, and retentive timers (in units of 8 points) • Timers have serial numbers.		• Usable with PC type A2A or A3H
	T256 to T2047	———	• 1792 points of 100 ms, 10 ms, and retentive timers (in units of 16 points) • Timers have serial numbers. • Setting devices ... D, R, W (Set values for the points exceeding 256 points)		• Usable with PC type A2A Unusable with PC type A3H
Setting of counter	Interrupt counter setting	———	• Set whether or not an interrupt counter (C224 to C255) is allocated for every point of the interrupt pointer.		• Usable with PC type A2A or A3H
	Number of used points	256 points (C0 to C255)	• 0 to 1024 points (in units of 16 points) • Setting devices ... D, R, W (Set values for the points exceeding 256 points)		• Usable with PC type A2A Unusable with PC type A3H
I/O number allocation		———	• 0 to 64 points (in units of 16 points) .....Input module/output module Special function module/vacant slot • Module type can be entered.		• Usable with PC type A2A or A3H PC type A3H cannot be registered.
Setting of remote RUN/PAUSE contact		———	• X0 to X1FF (A2AS), X0 to X3FF (A2AS-S1) (1 point for each of run and pause contacts.) • Setting of only pause contact cannot be performed.		• Usable with PC type~ A2A or A3H in the X's device range

Table 4.5 Parameter Setting Range List (Continued)

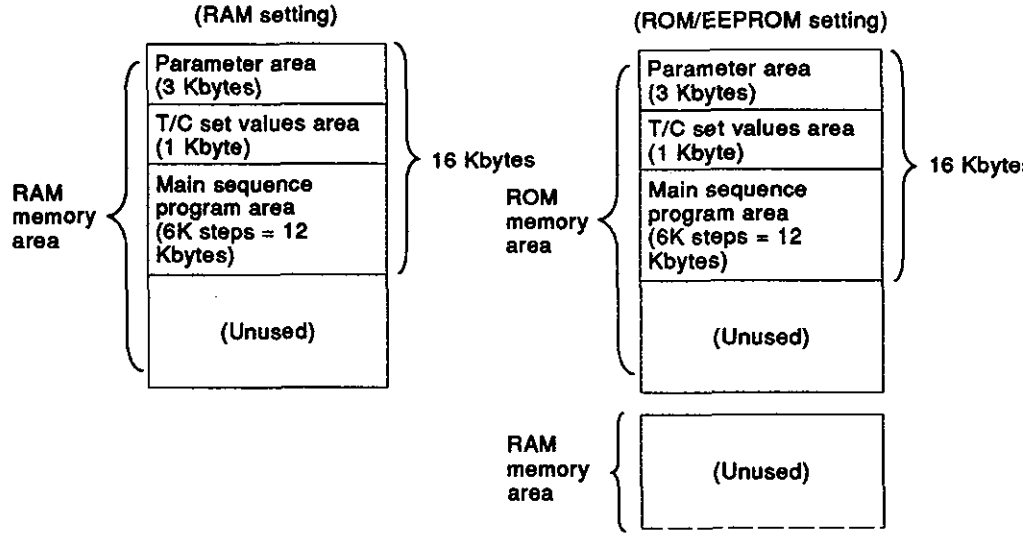
Item \ Setting		Default Value	Type		Remarks (Refer to Appendix 1.) (When existing software package is used.)
			A2ACPU	A2ASCPU-S1	
Operation mode at the time of error	Fuse blown	Continuation	Stop/continuation		• Usable with PC type A2A or A3H
	I/O verify error	Stop			
	Operation error	Continuation			
	Special function unit check error	Stop			
STOP → RUN display mode		Operation status prior to stop is re-output	Output before stop or after operation execution		• Usable with PC type A2A or A3H
Print title entry		———	• 128 characters		• Usable with PC types A2A or A3H
Keyword entry		———	• Max. 6 digits in hexadecimal (0 to 9, A to F)		• Usable with PC type A2A and A3H
MELSEC NET II link range setting	Number of link stations	———	• 0 to 64 stations		• Usable with PC type A2A • Unusable with PC type A3H, however, usable in the range of MELSECNET (BW0 to 3FF).
	Input/output (X/Y)		X/Y0 to 1FF (in units of 16 points)	X/Y0 to 3FF (in units of 16 points)	
	Link relay (B)		• B0 to BFFF (in units of 16 points)		
	Link register (W)		• W0 to WFFF (in units of 1 point)		
MELSECNET/MINI, MELSECNET/MINI-S3 link range setting		———	Number of support units: 0 to 8 units		• Usable with PC type A2A. • Unusable with PC type A3H
			Head I/O number: 0 to 1F0 (A2AS), 0 to 3F0 (A2AS-S1) (in units of 10^H)		
			Name entry: MINI, MINI-S3		
			Send/receive data: X, M, L, B, T, C, D, W, R, Absent (bit devices in units of 16 points)		
			Number of retries: 0 to 32 times		
			FROM/TO response specification: Link priority, CPU priority		
			Faulty station data clear specification: Retain/clear		
			Faulty station detection: M, L, B, T, C, D, W, R, Absent (bit devices in units of 16 points)		
			Error number: T, C, D, W, R		
			Total number of remote stations: 0 to 64 stations		
			Send status setting at line error: Test message, OFF data, retention (send data)		

4.4.2 User memory assignment

The memory areas of the built-in RAM and the memory cassette are assigned according to the parameter settings of the peripheral devices.
The parameters can be used only with the defaults, however, assign an memory area to them for effective use of the memory.
Only the memory areas to be assigned to the upgraded functions are different from those of the A1SCPU.

(1) Memory assignment without parameter settings (defaults)

(a) When no parameters are set, 16-Kbyte defaults are automatically assigned to the memory areas of the built-in RAM or ROM. The area for the sequence program is 6K steps or less, and empty areas are treated as unused.

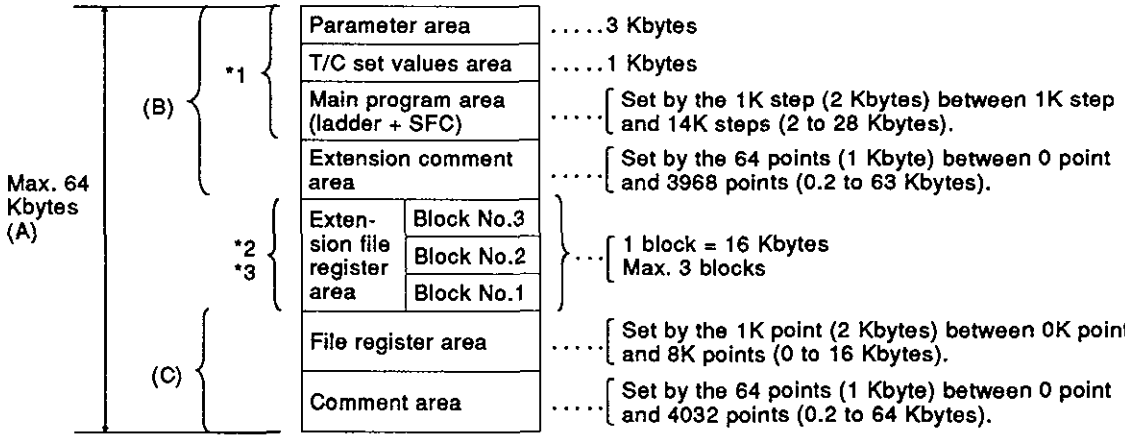


(2) Memory area assignment with memory settings

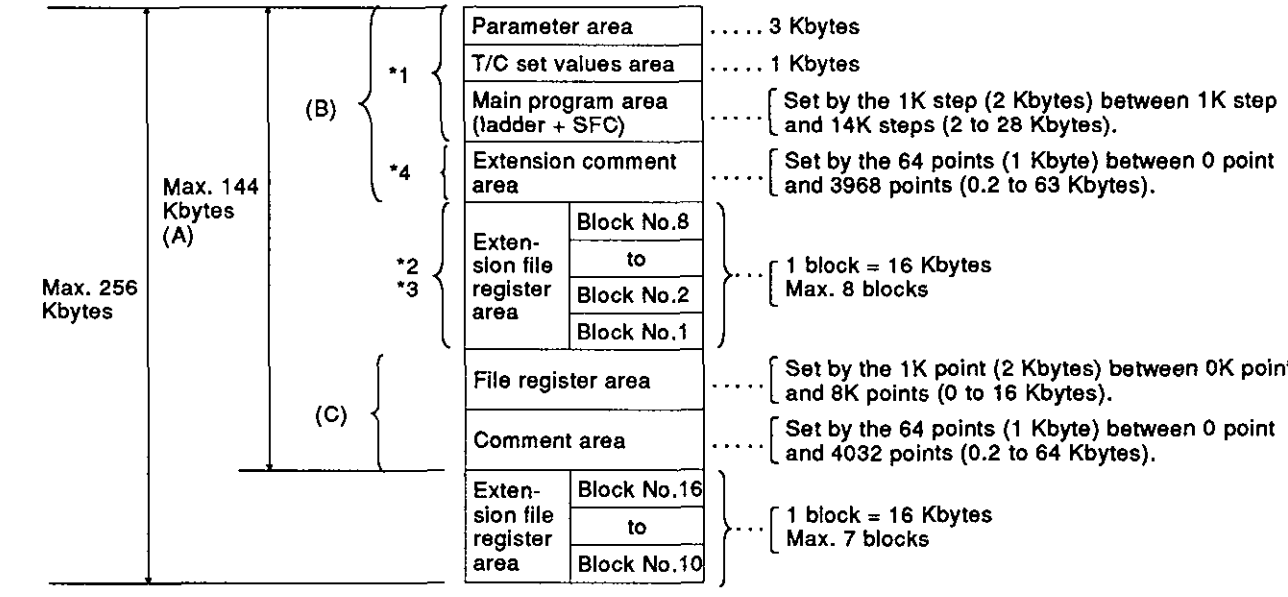
(a) When the built-in RAM and an A2SMCA-14KE are used

The memory areas are assigned as follows when the built-in RAM and an A2SMCA-14KE are used:

1) A2ASCPU (when the built-in RAM memory capacity is 64 Kbytes)



2) A2ASCPU-S1 (When the built-in RAM memory capacity is 256 Kbytes)



*1 For using an A2SMCA-14KE, this area can be used as ROM. Even so, the capacities of the extension comment, extension file register, file register and comment areas cannot be increased.

*2 Calculation of the number of available blocks in the extension file register area

$$\frac{(A)-(B)-(C)\ \text{Kbytes}}{16}=n$$

The integer of n represents the number of available blocks between block No.1 and No.8.

*3 In the sampling trace and status latch data storage areas, the extension file register block numbers are specified on-line.

*4 In setting extension comments, the memory capacity can be set up to 144 Kbytes plus extension comments (max. 63 Kbytes).
If the total memory capacity is over 144 Kbytes, the extension comments are stored in the extension file register area starting from block No.10. Once the extension comments have been stored in the blocks from No.10, the area indicated by *4 will turn into an empty area reserved for calculating the number of available blocks in the extension file register area with blocks No.1 to No.8.

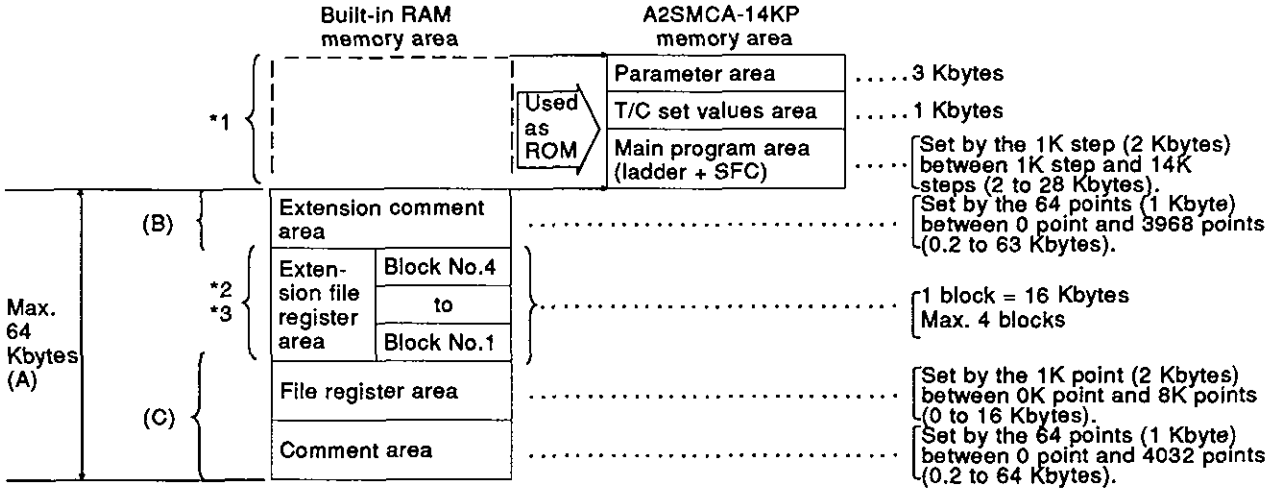
REMARK

If the total memory capacity set in parameters is over 64 Kbytes when an A2ASCPU (the built-in RAM memory capacity is 64 Kbytes) and an attempt at writing is made, the message "CAPACITY EXCEEDED. WRITING IMPOSSIBLE" will appear. Set parameters so that the total memory capacity will not be over 64 Kbytes.

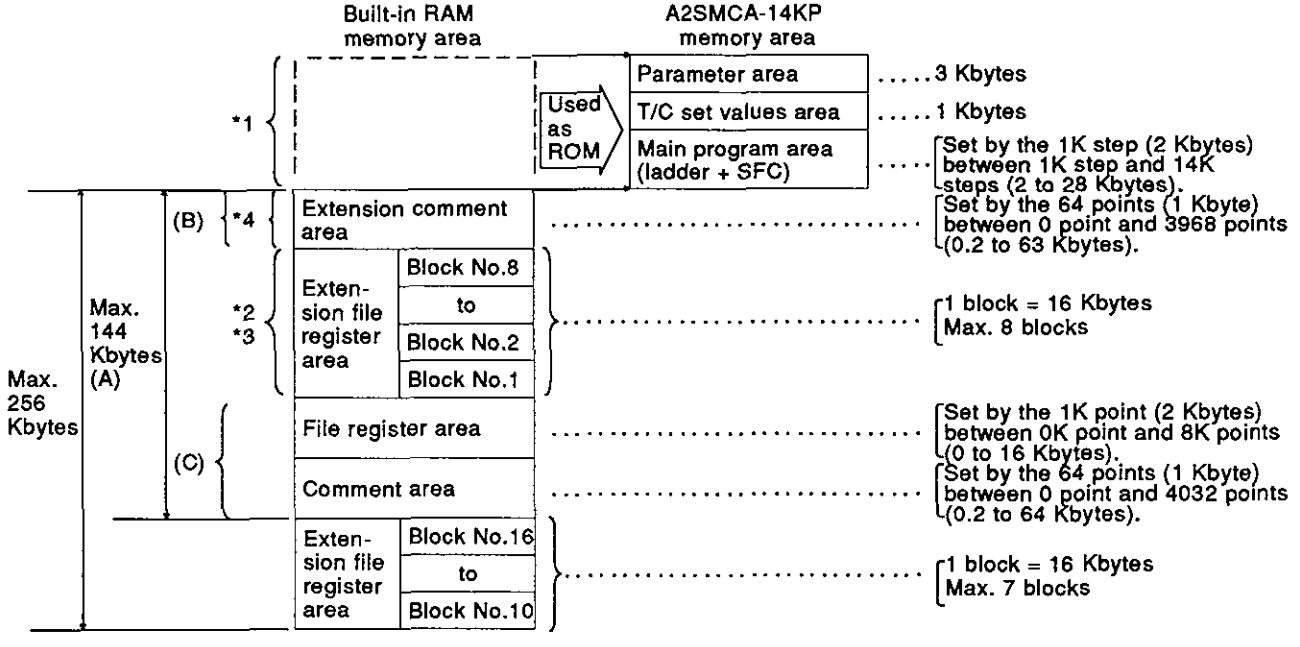
(b) When an A2SMCA-14KP is used

When an A2SMCA-14KP is used, the memory areas are assigned as shown below:

1) A2ASCPU (when the built-in RAM memory capacity is 64 Kbytes)



2) A2ASCPU-S1 (when the built-in RAM memory capacity is 256 Kbytes)



*1 For using an A2SMCA-14KP, this area can be used as ROM. By using the area in such a way, the capacities of the extension comment, extension file register, file register and comment areas can be increased.

For details of *2 to *4, see (a).

POINT

Functions using extension file registers and area reserving timing

The following describes the functions that use extension file registers, area reserving timing and area reserving priority.

Functions using extension file registers and area reserving timing

Function Using Extension File Registers	Area Reserving Timing	Area Reserving Priority
Extension comment	When writing parameters for setting the extension comment area capacity to the CPU.	1
SFC work area	When writing parameters for setting the microcomputer capacity to the CPU.	2
On-line sampling trace On-line status latch	When setting and writing trace/latch data storage register numbers to the CPU.	3
Extension file register access instruction Access via computer link	Check whether the corresponding block numbers are set and accessible when executing instructions or making access via computer link.	4

The SFC program work area uses block No. 2 of the default extension file register.
The work area may not be reserved when parameter settings or extension comments are stored in block No.10.
For details, see the MELSAP-II Programming Manual.

4.4.3 Timer and counter setting ranges

(1) Timer setting range

(a) Default values of the timer setting range are shown below.

Number of timer points	: 256 points
100 msec timer	: T0 to T199
10 msec timer	: T200 to T255
Retentive timer	: Absent

(b) Default values when setting the number of used timer points to 257 or more are shown below.

T0 to T199	: 100 msec timer
T200 to T255	: 10 msec timer
T256 to T2047	: 100 msec timer

(c) Timer types can be set as required by serial numbers in units of 8 points in the range of T0 to T255 and in units of 16 points in the range of T256 to T2047.

(d) The number of points used for the timer can be set as the number of timer points actually used in the sequence program. (Setting to 0 or multiples of 8 is possible.)

By setting to the number of timer points actually used, timer processing time after the END instruction can be shortened.

(e) Timer set values of T0 to T255 can be specified by constants or word devices; however, timer set values of T256 to T2047 should be specified by word device (D,W,R).

The timer set value cannot be specified by a constant.

Any required device must be allocated in parameter settings to word devices (D,W,R) to be used for storing timer set value of timers T256 to T2047.

(2) Counter setting range

(a) Default values of the counter setting range are shown below.

Number of counter points	: 256 points
Normal counter	: C0 to C255
Interrupt counter	: Absent

(b) Default values when setting the number of used counter points to 256 or more are shown below.

C0 to C255	: Normal counter
C256 to C1024	: Normal counter

(c) The counters which can be set as interrupt counters are within the range of C224 to C255. Counters outside this range cannot be set as interrupt counters.

Set interrupt counters in units of 1 point in the range of C224 to C255 using parameters.

Counters of C224 to C255 which are not set for interrupt counters can be used as normal counters.

Interrupt counters in the A2ASCPU count the number of interrupts I0 to I31.

Interrupt counters C224 to C255 are allocated to interrupt pointers I0 to I31 as shown below.

Interrupt Pointer	Interrupt Counter	Interrupt Pointer	Interrupt Counter	Interrupt Pointer	Interrupt Counter	Interrupt Pointer	Interrupt Counter
I0	C224	I8	C232	I16	C240	I24	C248
I1	C225	I9	C233	I17	C241	I25	C249
I2	C226	I10	C234	I18	C242	I26	C250
I3	C227	I11	C235	I19	C243	I27	C251
I4	C228	I12	C236	I20	C244	I28	C252
I5	C229	I13	C237	I21	C245	I29	C253
I6	C230	I14	C238	I22	C246	I30	C254
I7	C231	I15	C239	I23	C247	I31	C255

(d) The number of used counter points can be set as the actual number of counter points used in the sequence program. (Can be set to 0 points.)
By setting the actual number of counter points to be used, counter processing time after the END instruction can be shortened.

(e) Counter set values of C0 to C255 can be specified by constants or word devices; however, counter set values of C256 to C1023 should be specified by word device (D,W,R).
The counter set value cannot be specified by a constant.
Word devices to be used for storing set value counters C256 to C1023 must be allocated in parameter settings.

POINT

When the number of timer points is set to 257 or over or the number of counter points to 256 or over, the set value storage devices (D, R and W) specified when the number of timer and counter points to be used were set are automatically set in serial numbers.
<EX.>
When the set number of timer points is 512 and the set value storage device is D1000, the D devices (D1000 to D1255) will be given serial numbers and used for storing the set values for the 256 timers from T256 to T511.

4.4.4 MELSECNET/MINI-S3 automatic refresh

(1) To execute automatic communications with the batch refresh send/receive data buffer area of the A1SJ71PT32-S3/AJ71PT32-S3 master module, set automatic refresh for MELSECNET/MINI-S3 by using the peripheral device's parameter to write the setting to the A2ASCPU. When an error occurs in the MINI-S3, the error contents are automatically read out.

(2) The I/O devices allocated for send/receive operations by automatic refresh can be used to create a sequence program without modifications. (FROM/TO instructions are not necessary.)

POINTS

(1) Parameter setting for automatic refresh can be used to set up to 8 master modules, so that up to 8 modules can be handled with automatic refresh processing.
When 9 or more modules are used, use sequence program FROM/TO instructions.

(2) Automatic refresh is disabled with send/receive data for the partial refresh I/O modules and send/receive data for remote terminal module numbers 1 to 14. Use FROM/TO instructions to handle such data. However, the following remote terminal units are partly intended for automatic refresh;

- AJ35PTF-R2 RS-232C interface unit
- AJ35PT-OPB-M1-S3 operation box
- AJ35T-OPB-P1-S3 operation box

(3) The CPU automatically turns ON the link communications start signal Y(n+18) or Y(n+28) for the master modules set with automatic refresh. It is not necessary to turn the signal ON by using the sequence program.

(4) Automatic refresh of I/O data is processed in batch after the END instruction execution.

(3) The parameter setting items, setting ranges, and contents for automatic refresh are as given in the table below.
Perform parameter setting the number of times equal to the number of A1SJ71PT32-S3/AJ71PT32-S3 master modules.

Table 4.6 Automatic Refresh Parameter Setting Ranges, Items, and Contents

No.	Item	Setting range	Description
1	Number of master modules	1 to 8 modules	• Set the total number of used master units.
2	Head I/O *number*	I/O points of CPU	• Set the head I/O number with which the master unit is installed.
3	Name entry	• MINI or MINI-S3	• MINI ... for I/O dedicated mode (32 points occupied) • MINI-S3 ... for extension mode (48 points occupied)
4	Total number of remote I/O stations	0 to 64 stations	• Set only when MINI is used. • This setting is not necessary when MINI-S3 is used since the number of the initial ROM of the master modules is effective. (Ignored when set.)
5	Receive data storage device	• X • M, L, B, T, C, D, W, R, absent (bit devices in units of 16 points)	• Set the devices to store batch refresh send/receive data. • Set the head device number. • The area equal to the number of stations beginning with the head device is occupied as the automatic refresh area. (8 points/station x 64 stations = 512 points .... bit devices) • *Use of X/Y for remote I/O range is recommended.*
6	Send data storage device	• Y • M, L, B, T, C, D, W, R, absent (bit devices in units of 16 points)	
7	Number of *retries*	0 to 32 times	• Set the number of retries to be made when a communication error occurs. • *Error is not output when communication is restarted within the set number of the retries.*
8	FROM/TO response *specification*	Link priority, CPU priority (Select the access to the *master unit buffer memory.*)	(1) Link priority ... Priority is given to the MINI-S3 link access FROM/TO instructions are kept *waiting during link access.* • Refreshed receive data can be read at the same timing. • Max. waiting time (0.3 msec + 0.2 msec x number of partial refresh stations) for FROM/TO instructions will be provided. (2) CPU priority ... Priority is given to CPU's FROM/TO instruction access. This access interrupts in the link access. • Depending on timing, received data being refreshed may be read out. • No waiting time for FROM/TO instructions.

Table 4.6 Automatic Refresh Parameter Setting Ranges, Items, and Contents (Continued)

No.	Items	Setting range	Description
9	Faulty station data clear specification	Retain/clear (receive data)	•Retain ... Retains data for batch/partial refresh. •Clear ... All points set to OFF.
10	Faulty station detection	M, L, B, T, C, D, W, R, absent (bit devices in units of 16 points)	•Set the head device to store faulty station detection data. •MINI ... 4 words, MINI-S3 ... 5 words are occupied.
11	Error number	T, C, D, W, R	• Set the head device to store error code when an error occurs. •MINI ... 1 word, MINI-S3 ... (1 + number of remote terminals) words
12	Line error check setting (line error)	• Sending test message • Sending OFF data •Sending data immediately before a line error occurrence	•Set the data communications method to check faulty position when an line error occurs.

POINTS

(1) Refer to the following manual for details of MELSECNET/MINI-S3.

- AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual
- A1SJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

(2) Refer to the operating manuals of the peripheral devices for parameter setting methods.

4.5 Operation Processing Methods

This section describes A2ASCPU operation processing.

4.5.1 Stored program repeat operations system

This A2ASCPU operation processing method is a stored program repeat operations system. This is shown in Fig. 4.2.

(1) Stored program system

(a) The user program system for executing operations is stored in the CPU memory areas in the PC. In operation execution, instructions in the stored program are serially read to the CPU and, according to the execution results of these instructions, the status of each device is controlled.

(b) The stored program system is a system of storing the user program to CPU memory areas in advance.

(2) Repeat operations system

(a) The PC executes the program stored in CPU memory areas in order from step 0 to the END (FEND) instruction. After End (FEND) instruction execution, the present values of the timer and counter are updated, internal processing such as self-diagnostic check are executed, and the program is returned to step 0.

The system which repeatedly executes this series of processing is referred to as the repeat operations system.

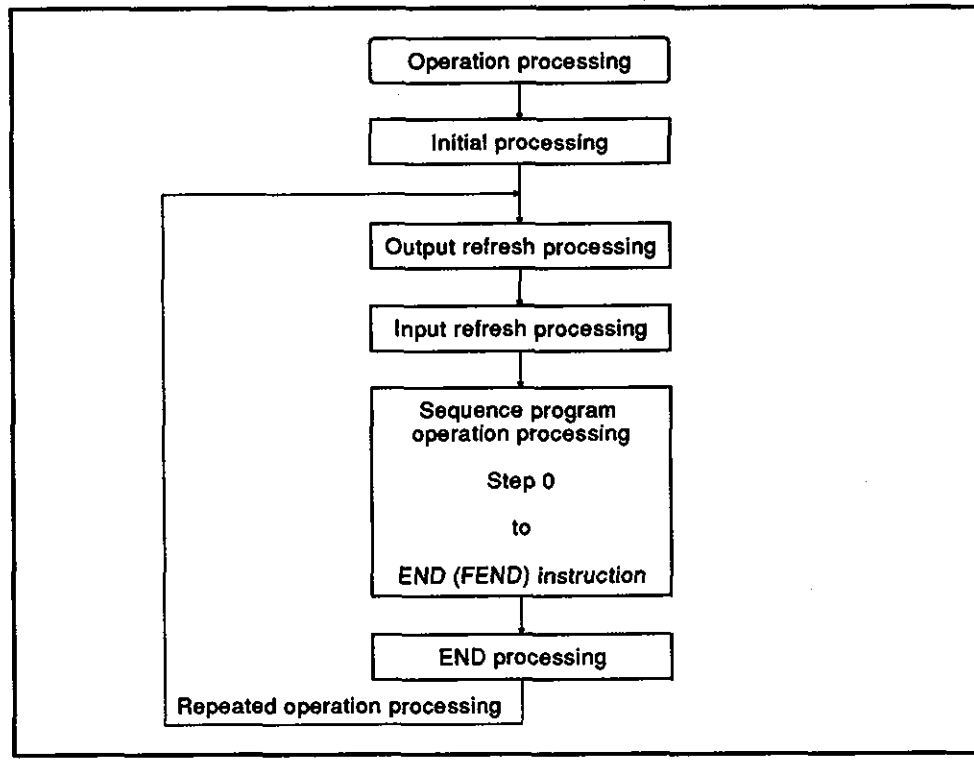


Fig.4.1 Repeated Operation Processing

4.5.2 Initial processing

Initial processing starts the sequence program operation. Initial processing is carried out when the PC CPU power supply is turned on or when the RESET switch of the PC CPU is pressed. The following processes are executed during initial processing.

The initial processing time is 2 to 3 seconds, depending on system configuration.

(1) I/O modules initialization

Resets and initializes the I/O modules.

(2) Data memory clear

(a) Clears the data memory unlatched.

The latched data memory area is set with a single parameter from the peripheral device.

(b) Clears Y if Y corresponding to the areas occupied by input modules and not occupied by any module are used as internal relays M.

(3) Link parameter setting

When the A2ASCPU is used as the master station in MELSECNET(II), set the link parameter data to the data link module to initiate data link.

(4) I/O address allocation

Allocates I/O addresses to the I/O modules loaded on the base unit. For further details, see Section 4.8.1.

(5) I/O modules data entry

Enters the types of I/O modules loaded on the base unit.
I/O module data is used to verify the I/O modules.

(6) Self-diagnosis

The PC CPU conducts self-checks when it is powered up or reset. For details, see Section 4.3.1.

4.5.3 END processing

Returns the PC CPU to step 0 in the repeated operation processing.
The following processing are performed after the [END] (FEND) instruction is executed.

(1) Self-diagnosis

Checks for fuse blown, I/O modules verify error, battery power reduction, *etc.*
For further details, see Section 4.3.1.

(2) Timer/counter processing.

Updates timer/counter present values and contact status.

(3) Constant scan processing

Allows the repeated operation processing to be initiated after the specified constant scan time (set to special data register D9020).

(4) Data communication processing with data access unit

Data transfer is executed between PC CPU and data access unit when data transfer is requested by a data access unit such as computer link module.

(5) Link refresh processing

Executed when a link refresh request is made by a link module.

(6) Sampling trace processing

Stores the specified device status to the sampling trace area when the sampling trace is executed every scan (after END execution).

(7) RUN/STOP switch position check

Changes the PC CPU operating status in accordance with the RUN/STOP switch position.
For transition processing to the RUN, STOP, PAUSE and STEP-RUN actions, see Section 4.5.5.

4.5.4 Operation processing at momentary power failure occurrence

The PC CPU detects any momentary power failure when the input line voltage to the power supply module falls below the defined value.

When the PC CPU detects any momentary power failure, the following operations will be executed.

(1) Momentary power failure within 20 msec

(a) The operation processing is stopped with the output retained.

(b) The operation processing is resumed when normal status is restored.

(c) The watchdog timer (WDT) keeps timing while the operation is at a stop.
For example, if a momentary power failure of 15 msec occurs when the scan time is 190 msec, a watchdog timer error (200 msec) results.

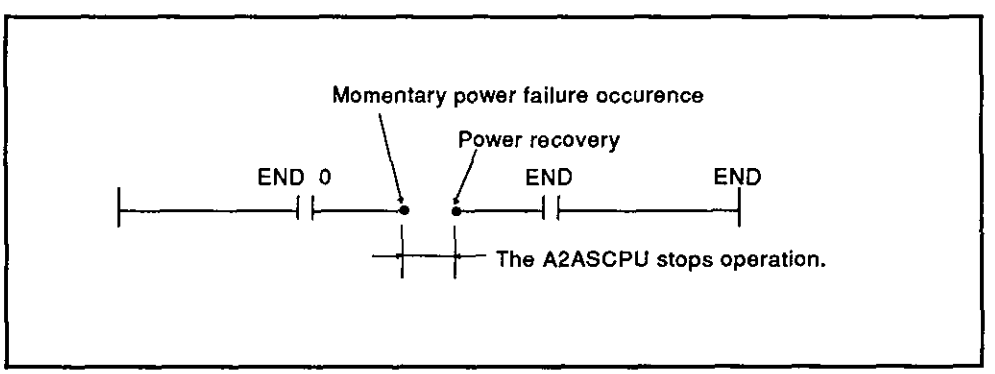


Fig. 4.2 Operation Processing at Occurrence of Momentary Power Failure

(2) When a momentary power failure exceeds allowable momentary power failure time

The PC CPU is reset to the initial start state.

This state allows operation processing which is the same as that when the power is turned ON or the CPU is reset by using the reset switch.

REMARK

The momentary power failure time is different depends on used power supply module. Refer to section 6.1.1.

4.6 RUN, STOP, PAUSE, STEP-RUN Operation Processing

The PC CPU is operated in the RUN, STOP, PAUSE and STEP-RUN states as described below.
The following describes the PC CPU operation processing in specific operation states.

(1) RUN operation processing

(a) RUN indicates repeated operation of the sequence program in order of step 0 to END(FEND) instruction.

(b) When the CPU enters the RUN state, the output state saved at the time of STOP is output according to the STOP → RUN output mode setting made with parameters.

(c) The processing time required until the sequence program operation starts after STOP to RUN switching is usually 1 to 3 seconds including a little variation due to the system configuration.

(d) The processing mentioned in (6) is repeated until the RUN state is switched to another state.

(2) STOP operation processing

(a) STOP indicates a stop of the sequence program operation by using the RUN/STOP switch or remote STOP (see Section 4.3).

(b) When the CPU is set to STOP, the output status is saved and all outputs are switched OFF. Data other than outputs (Y) is retained.

(c) The processing mentioned in (6) is repeated until the STOP state is switched to another state.

(3) PAUSE operation processing

(a) PAUSE indicates a stop of the sequence program operation with the output and data memory status retained (see Section 4.3).

(b) The processing indicated in (6) is repeated until PAUSE is switched to another state.

(4) STEP-RUN operation processing

(a) STEP-RUN indicates a RUN mode which allows the sequence program operation processing to be stopped or continued per instruction by using the peripheral device (see Section 4.3).

(b) The execution state can be checked as the operation processing is stopped with the output and data memory status retained.

(c) The processing indicated in (6) is repeated until STOP-RUN is switched to another state.

(5) PC CPU operation processing by RUN/STOP key switch shifting

PC CPU Operation Processing / RUN/STOP Key Switch Shifting	Sequence Program Operation Processing	External Output	Data Memory (Y, M, L, S, T, C, D)	Remarks
RUN→STOP	The operation continues to the END instruction and stops.	The OS saves the output status and turns OFF all outputs.	The status right before the STOP state is retained.	
STOP→RUN	The operation starts.	The output depends on the output mode of the parameter when shifting the key switch from STOP to RUN.	The operation restarts from the point right before the STOP state.	

(6) Operation processing by RUN/STOP key switch shifting

Processing / RUN /STOP Key Switch Position	I/O Refresh (In Refresh Mode)	Self-diagnosis Check	Timer/counter Current Value Updating And Contact On/Off	Constant Scan (when Constant Scan is Set)	Computer Link Unit Data Communication	Link Refresh	Sampling Trace	RUN/STOP Key Status Check	Remarks
RUN (END processing)	Executed	Executed	Executed	Executed	Executable	Executable	Executed	Executed	
STOP	Executed	Executed	—	—	Executable	Executable	—	Executed	

(7) Processing by key switch shifting in response to requests from peripheral devices

Key Switch Position / CPU Operation Processing / Request from peripheral device		RUN			STOP
		Sequence Program Operation Processing	External Output	Data Memory (Y, M, L, S, T, C, D)	—
Request on sequence program by parameter setting	RUN contact ON	The operation continues to the END instruction and stops.	The OS saves the output status and turns OFF all outputs.	The status right before the STOP state is retained.	RUN not executable
	PAUSE contact ON (when M9040 is ON)	The operation stops at the step specified by the peripheral device.	The output status is retained.	The operation restarts from the point right before it was suspended.	PAUSE not executable
Request from peripheral device's PC test function	PAUSE (when M9040 is ON)	The operation continues to the END processing and stops.		The status right before the PAUSE state is retained.	PAUSE not executable
	STEP-RUN	The operation stops at the step specified by the peripheral device.		The operation restarts from the status right before it was suspended.	STEP-RUN not executable

4.7 Special Function Module I/O Allocation

By registering the types of the following special function modules during I/O allocation by peripheral devices, dedicated instructions associated with the modules can be used.

Special Module	Type	Type to be registered
High speed counter module	AD61 (S1)	AD61
Memory card/Centronics interface module	AD59 (S1)	AD59
Computer link module (no-protocol mode)	AJ71C24 (S3, S6, S8)	C24S3
	AJ71UC24	C24
	A1SJ71C24 (R2, PRF, R4)	C24
Terminal interface module	AJ71C21 (S1)	C21
MELSECNET/MINI-S3 data link module	AJ71PT32-S3	PT32S3
	A1SJ71PT32-S3	PT32S3
CRT/LCD controller module	AD57 (S1)	AD57 (S1)
	AD58	AD58

4.8 Handling Instructions

(1) Do not subject the CPU module and memory cassette to impact or shock.

(2) Do not remove printed circuit boards from the housing. There are no user-serviceable parts on the boards.

(3) Ensure that no conductive debris can enter the module. If it does, make sure that it is removed. Guard particularly against wire offcuts.

(4) Tighten the module mounting and terminal screws as specified below.

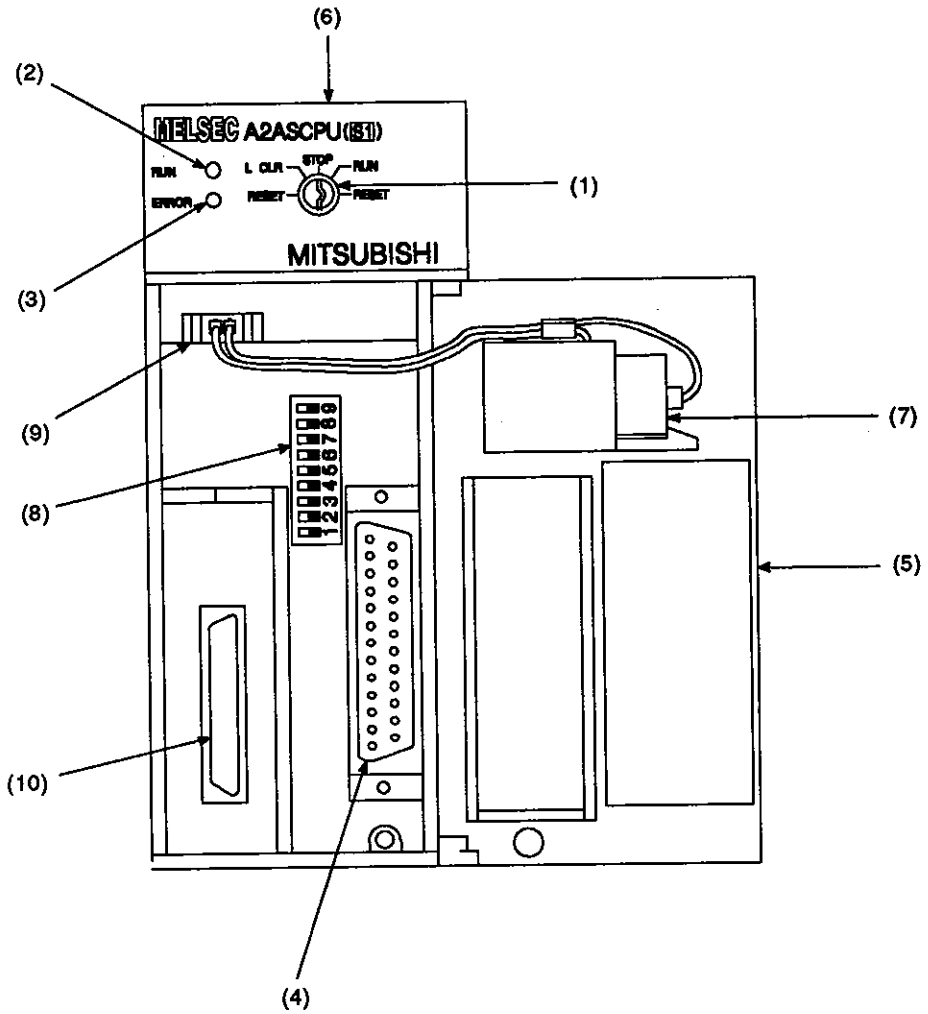
Screw	Tightening Torque N.cm [kg.cm] (lb.inches)
Module terminal block installation screws (M4)	98 [10] (8.66) to 137 [14] (12.13)
Module mounting screws (M4)	78 [8] (6.93) to 118 [12] (10.39)

(5) To load the module onto the base, hook the two lower lugs into the cut out and gently swing the module into place. Ensure that the top catch engages. To remove, press the top catch and swing the module out before unhooking the lower lugs. (See Section 9.5 for detail.)

MEMO

4.9 Part Identification and Setting of A2ASCPU

4.9.1 Part identification

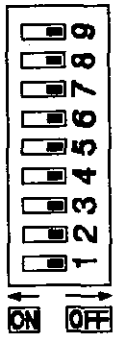


No.	Name	Function
(1)	RUN/STOP key switch	• RUN/STOP : To start/stop running a sequence program. • RESET : To reset the hardware. To reset an error occurring during operation to initialize operation • LATCH CLEAR (L-CLR) : To clear (turning OFF, or clearing to "0") the devices in the latch range and non-latch range which are set by parameters. For the latch clear operation procedure, refer to Section 4.9.3.

No.	Name	Function
(2)	"RUN" LED	• ON : A sequence program operation is being executed with the RUN key switch set in the RUN position. (The LED remains lit if an error (Section 11.3), which permits sequence operation to continue, occurs.) • OFF : The RUN LED goes out in the following cases. • 100/200 VAC is not supplied to the A2ASCPU. • The RUN key switch is in the STOP position. • The remote STOP signal is input. • The remote PAUSE signal is input. • Flashing : The RUN LED flashes in the following cases. • An error which causes sequence operation to stop is detected by the self-diagnosis function. • The latch clear operation is executed.
(3)	"ERROR" LED	• ON : The self-diagnosis function detects an error. (When the detected error is set to "not lit" in the ERROR LED indication priority setting) • OFF : No error occurs or a malfunction is detected by the [CHK] instruction. • Flashing : An annunciator (F) is turned ON by the sequence program.
(4)	RS-422 connector	• Used to connect a peripheral device to write/read, monitor, or test a program with a peripheral device. • Close with the cover when not connected to a peripheral device.
(5)	Cover	• Protects A2ASCPU printed circuit board, memory cassette, RS-422 connector, battery, etc • Execute the following operations with the cover open. • Memory cassette connection/disconnection • Setting a dip switch • Connection to battery connector • For mounting the module to the base unit battery replacement
(6)	Module fixing screws	• For mounting the module to the base unit
(7)	Battery	• For refaining the base unitretains data such as programs, device latch ranges, file registers, etc. (See 8.2 for battery replacement.)
(8)	Dip switch	• Used for setting the memory-protect function. (See sections 4.9.2)
(9)	Battery connector	• For connection to the battery
(10)	Memory cassette installing connector	• For installing the memory cassette (A2ASMCA-14KP/14KE) (With a memory cassette installed, ROM automatically becomes available.)

4.9.2 Memory protect switch setting

The memory protect switches are used for protecting RAM memory data from being overwritten by accidental incorrect operation of peripheral device. (When the CPU equipped with a memory cassette is operated using ROM or EEPROM, the memory switch settings will be invalid.)
The function prevents overwriting and deleting of the program once it has been written.
To change the contents of RAM memory, turn OFF all the memory protect switches.
The switches are OFF when delivered.



Memory Protect Range (Kbytes)	Setting Switch	
	A2ASCPU	A2ASCPU-S1
0 to 16	Turn ON switch 1.	Turn ON switch 1.
16 to 32	Turn ON switch 2.	Turn ON switch 2.
32 to 48	Turn ON switch 3.	Turn ON switch 3.
48 to 64	Turn ON switch 4.	Turn ON switch 4.
64 to 80	Unused	Turn ON switch 5.
80 to 96	Unused	Turn ON switch 6.
96 to 112	Unused	Turn ON switch 7.
112 to 144	Unused	Turn ON switch 8.
144 to 256	Unused	Turn ON switch 9.

POINTS

(1) For using the memory protect function, check the addresses (step numbers) in each memory area (sequence program, comment, sampling trace, status latch and file register) to set the switches.

(2) Do not use the memory protect function for the data storage areas when either a sampling trace or a status latch is executed. If used, the data executed cannot be stored in memory.

REMARK

When an A2SMCA-14KE is used, the memory protect function is available with its memory protect setting pins. See Section 8.1.4.

4.9.3 Latch clear

To clear the latch using the RUN/STOP switch, follow the steps described below. Once it is cleared, the unlatched devices will be also cleared.

(1) Turn the RUN/STOP switch from the "STOP" position to the "L.CLR" position several times to make the "RUN" LED start flashing at very short intervals (ON for approx. 0.2 second and OFF for 0.2 second). The quickly flashing LED indicates that the preparations for latch clear have been completed.

(2) After the "RUN" LED has started flashing quickly, again turn the RUN/STOP switch from the "STOP" position to the "L.CLR" position. Latch clear will be completed, and the "RUN" LED will go off.
To cancel latch clear, turn the RUN/STOP switch to the "RUN" position to bring the A2ASCPU into the RUN status, or to the "RESET" position to reset the A2ASCPU.

REMARK

Latch clear can be executed by the GPP function.
Latch clear by an A6GPP, for example, is achieved by "Device All Clear" of the PC mode test function.
For details of operation, see the operating manual covering the GPP function.

5. POWER SUPPLY MODULE

5.1 Specifications

5.1.1 Power supply specifications

Table 5.1 shows the specifications of power supply modules.

Table 5.1 Power Supply Module Specifications

Item		Specifications		
		A1S61P	A1S62P	A1S63P
Base loading position		Power supply module loading slot		
Input voltage		100 to 120 VAC$^{+10\%}_{-15\%}$ (85 to 132 VAC)		DC24V$^{+30\%}_{-35\%}$ (15.6 to 31.2 VDC)
		200 to 240 VAC$^{+10\%}_{-15\%}$ (170 to 264 VAC)		
Input frequency		50/60 Hz ±3 Hz		—
Max. input apparent power		105 VA		41W
Input current		20A within 8 msec		81A within 1 msec
Rated output *current*	5 VDC	5 A	3 A	5A
	24 VDC±10%		0.6 A	
*1 Overcurrent protection	5 VDC	5.5 A or higher	3.3 A or higher	5.5 A or higher
	24 VDC		0.66 A or higher	
*2 Overvoltage protection	5 VDC	5.5 to 6.5 V	5.5 to 6.5 V	5.5 to 6.5 V
	24 VDC		—	
Efficiency		65% or higher		
Power indicator		Power LED display		
Terminal screw size		M3.5 x 7		
Applicable wire size		0.3 to 2 mm^2		
Applicable solderless terminal		V1.25-3.5, V1.25-YS3A, 2-3.5, 2-YS3A V1.25-M3, V2-YS3A, V2-S3, V2-YS3A		
Applicable tightening torque		6 to 9 kg/cm		
External dimensions mm (inch)		130 x 55 x 94 (5.12 x 2.17 x 3.70)		
Weight kg (lb)		0.53 (1.17)	0.55 (1.21)	0.5 (1.1)
*3 Allowable momentary power failure time		within 20 msec		within 1 msec

POINTS

*1 : Overcurrent protection

The overcurrent protection device shuts off the 5V, 24 VDC circuit and stops the system if the current flowing in the circuit exceeds the specified value.
When this device is activated, the power supply module LED is switched OFF or dimly lit. In this case, remove any cause of overcurrent and start up the system.

*2 : Overvoltage protection

The overvoltage protection device shuts off the 5 VDC circuit and stops the system if 5.5 to 6.5 V voltage is applied to the circuit.
When this device is activated, the power supply module LED is switched OFF. In this case, switch OFF, then ON the input power to restart the system.
The power supply module must be changed if the system is not booted and the LED remains OFF.

*3 : Allowable momentary power failure time

This value indicates the momentary power failure time allowed for the PC CPU and varies according to the power supply module used with the PC CPU module.
The allowable momentary power failure time for a system in which an A1S63P is used is defined that it starts when the primary power supply of the 24 VDC stabilized power supply of the A1S63P is turned OFF and lasts until the 24 VDC becomes less than the specified voltage (15.6 VDC).

5.1.2 Selection of power supply module

Select the power supply module according to the total current consumption of I/O modules, special-function modules, and peripheral device supplied by that power supply module. When the extension base A1S52B(S1), A1S55B(S1), A1S58B(S1), A55B or A58B is used, power is supplied from the power supply module of main base. Therefore, this points should also be taken into consideration.

Section 2.3 gives the details of I/O module, special-function module, and 5 VDC current consumption of a peripheral device.

(1) When extension base A1S52B(S1), A1S55B(S1), A1S58B(S1), A55B or A58B is used, the 5 VDC power is supplied from the power supply module of the main base unit via the extension cable. Therefore, when the A1S52B(S1), A1S55B(S1), A1S58B(S1), A55B or A58B is used, note the following points:

(a) Select 5 VDC capacity of power supply module in the main base unit so that in can cover the current consumption of 5 VDC use for the A1S52B(S1), A1S55B(S1), A1S58B(S1), A55B or A58B.

Example:

Assuming that the 5 VDC current consumption of main base unit is 3 A and the 5 VDC current consumption of A1S55B(S1) is 1 A, it is required to select the A61P(5 VDC, 5 A) for the power supply module on the main base unit.

(b) Since the power supplied to the A1S52B(S1), A1S55B(S1), A1S58B(S1), A55B or A58B via the extension cable, some voltage drop occurs over the cable. It is necessary to select the power supply module and cable length which provide 4.75 VDC or more at the receiving end.

For details of voltage drop. etc., refer to Section 7.1.3 "Application standards of extension base unit".

5.2 Handling

This section gives handling instructions, PC nomenclature and hardware setting instructions.

5.2.1 Handling instructions

(1) Do not subject supply module and memory cassette to impact or shock.

(2) DO not remove printed circuit boards form the housing. There are no user-serviced parts on the boards.

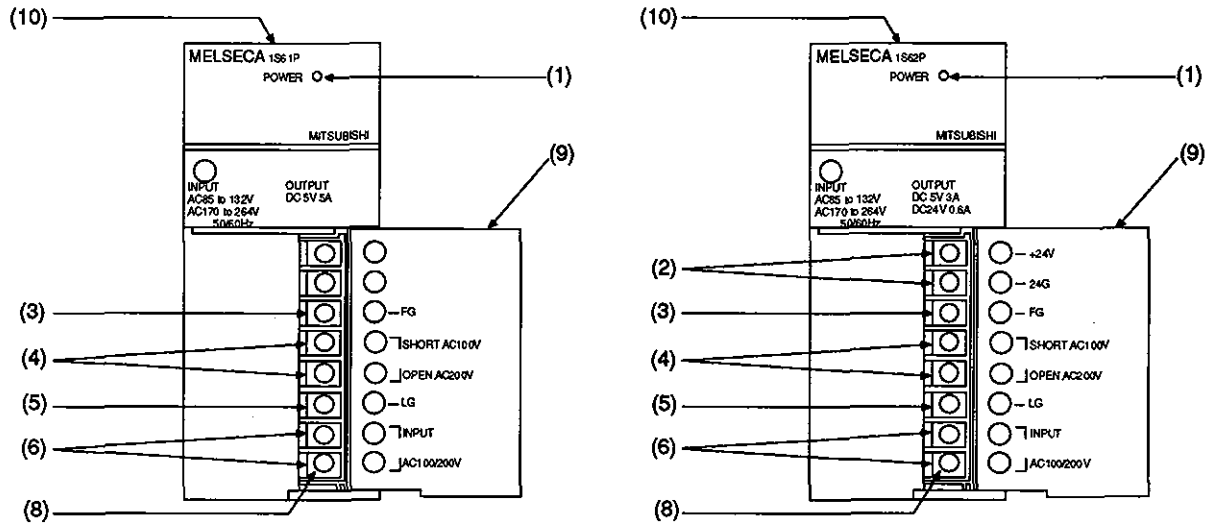
(3) Ensure that no conductive debris can enter the module. If it does, make sure that it is removed. Guard particularly against wire offcuts.

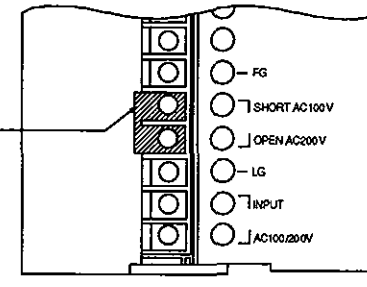
(4) Tighten the module mounting and terminal screws as specified below.

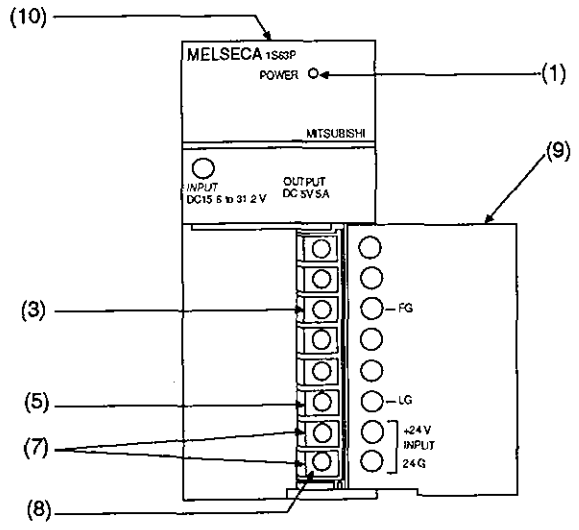
Screw		Tightening Torque N·cm [kg·cm] (lb·inches)
Power supply module terminal block terminal screw	(M3.5)	59[6](0.24) to 88[9](0.35)
Module mounting screws	(M4)	78[8](6.93) to 118[12](10.39)

5.3 Names and Purposes of Parts and Settings

The names and purposes of parts of the power supply module are described below.



No.	Name	Purpose
(1)	POWER LED	Used to indicate the 5 VDC power supply.
(2)	24 VDC and DC24G terminals	Used to supply the 24 VDC power to the output module as the internal power supply. (supplied by an external wire)
(3)	FG terminal	Grounding terminal connected to the shield pattern on the PC board.
(4)	Operating voltage switching terminals	Used to switch the input voltage. Connect these terminals with a shorting strip when a 100 VAC power is supplied. Leave these terminals open when a 200 VAC power is supplied.
		<Setting when a 100 VAC power is supplied> Connect these terminals with a shorting strip (supplied with the module). 



No.	Name	Purpose
(5)	LG terminal	Used to ground the power supply filter. Provided with a potential half the input voltage.
(6)	Power input terminal	Used to connect to 100 or 200 VAC power supply.
(7)	Power input terminal	Used to connect to a 24 VDC power supply.
(8)	Terminal screw	M3.5 x 7
(9)	Terminal cover	Used to protect the terminal block.
(10)	Module mounting screw	Used to secure the module to the base unit.

POINT

If the power supply voltage setting is different from actual power supply voltage, the following problem will occur.

	Power Supply Voltage	
	100 VAC	200 VAC
Setting for 100 VAC (the operating voltage switching terminals are shorted)	——	The power supply module will be destroyed. (The CPU will not cause problem.)
Setting for 200 VAC (the operating voltage switching terminals are open)	The power supply module will not cause problem. The CPU will not operate.	——

6. BASE UNIT AND EXTENSION CABLE

6.1 Specifications

6.1.1 Specifications of base units

(1) Specifications of main base units

Table 6.1 Main Base Unit Specifications

Item \ Model	A1S32B	A1S33B	A1S35B	A1S38B
Loaded I/O modules	2 can be loaded	3 can be loaded	5 can be loaded	8 can be loaded
Extension connection	Enabled			
Installation hole size	φ6-mm (0.24 inch) slot (for M5 screw)			
External dimensions mm(in)	220 x 130 x 28 (8.66 x 5.12 x 1.10)	255 x 130 x 28 (10.04 x 5.12 x 1.10)	325 x 130 x 28 (12.80 x 5.12 x 1.10)	430 x 130 x 28 (16.93 x 5.12 x 1.10)
Weight kg(lb)	0.52 (1.14)	0.65 (1.43)	0.75 (1.65)	0.97 (2.13)
Accessory	Four mounting screws (M5 x 25)			

(2) Specifications of extension base units

Table 6.2 Extension Base Unit Specifications

Item \ Model	A1S65B(S1)	A1S68B(S1)	A1S52B(S1)	A1S55B(S1)	A1S58B(S1)
Loaded I/O modules	5 can be loaded	8 can be loaded	2 can be loaded	5 can be loaded	8 can be loaded
Power supply module loading	Required		Not required		
Installation hole size	φ6-mm (0.24 inch) slot (for M5 screw)				
Terminal screw size	—	—	M4 x 6 (FG terminal)		
Applicable wire size	—	—	0.75 to 2 mm^2		
Applicable solderless terminal size	—	—	(V)1.25-4, (V)1.25-YS4, (V)2-YS4A (Applicable tightening torque: 12 kg/cm (67.1 lb/inch)		
External dimensions mm(inch)	315 x 130 x 28 (12.40 X 5.12 X 1.10)	420 x 130 x 28 (16.54 X 5.12 X 1.10)	135 x 130 x 28 (5.31 X 5.12 X 1.10)	260 x 130 x 28 (10.24 X 5.12 X 1.10)	365 x 130 x 28 (14.37 X 5.12 X 1.10)
Weight kg(lb)	0.71 (1.56)	0.95 (2.09)	0.38 (0.84)	0.61 (1.34)	0.87 (1.91)
Accessory	Four mounting screws (M5 x 25)		*1 One dustproof cover (for I/O module) Four mounting screws (M5 x 25)		

*1: For the installation of the dustproof cover, see Section 9.6.

POINT

When using either base unit A1S52B(S1), A1S52B(S1) or A1S58B(S1) which do not require supply module, refer to Section 5.1.2 "Selection of power supply module" and Section 6.1.3.

6.1.2 Specifications of extension cables

Table 6.3 shows the specifications of extension cables which can be used for the A2ASCPU system.

Table 6.3 Extension Cable Specifications

Item \ Model	A1SC01B	A1SC03B	A1SC12B	A1SC30B	A1SC60B	A1SC05NB	A1SC07NB
Cable length m(ft)	0.055 (0.18)	0.33 (1.08)	1.2 (3.94)	3.0 (9.84)	6.0 (19.68)	0.45 (1.48)	0.7 (2.3)
Resistance value of 5 VDC supply line (Ω at 55 °C)	0.02	0.021	0.055	0.121	0.182	0.037	0.045
Application	Connection between main base unit and A1S5[ ]B(S1)/A1S6[ ]B(S1)					Connection between main base unit and A5[ ]B/A6[ ]B.	
Weight kg(lb)	0.025 (0.055)	0.01 (0.022)	0.20 (0.44)	0.4 (0.88)	0.65 (1.43)	0.2 (0.44)	0.22 (0.48)

6.1.3 Application standards of extension base unit (A1S52B(S1), A1S55B(S1), A1S58B(S1), A55B, A58B)

When an extension base unit of models A1S52B(S1), A1S55B(S1), A1S58B(S1), A55B, or A58B is used, make sure a voltage of 4.75 V or above is supplied to the receiving end (at the module installed in the last slot of the extension base unit).

With the A1S52B(S1), A1S55B(S1), A1S58B(S1), A55B, or A58B extension base unit, 5 VDC is supplied from the power supply module of the main base unit via extension cable. Therefore, some voltage drop occurs over the extension cable and the specified voltage is not supplied to the receiving end, resulting in mis-input and mis-output.

If the voltage at the receiving end is less than 4.75 V, use an extension base unit of models A1S65B(S1), A1S68B(S1), A65B, or A68B equipped with a power supply unit.

(1) Selection conditions

The voltage received by the module installed in the last slot of an extension base unit A1S52B(S1), A1S55B(S1), A1S58B(S1), A55B, or A58B must be 4.75 V or above.

Since the output voltage of the power supply module is set at 5.1 V or above, the voltage drop must be 0.35 V or less.

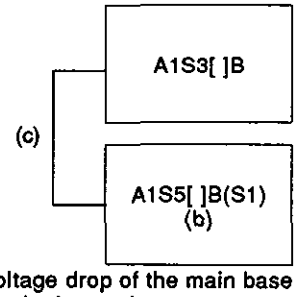
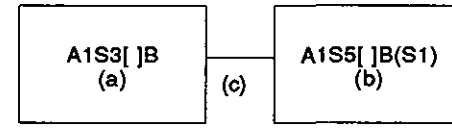
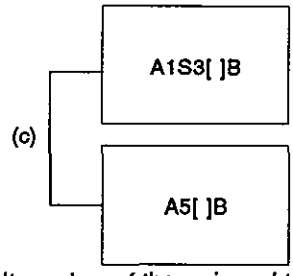
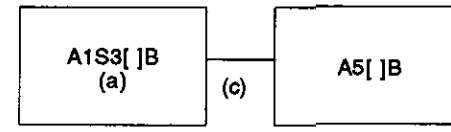
(2) Classification of voltage drop

Voltage drop is classified into (a), (b), and (c) as follows according to the connecting method and type of extension base units.

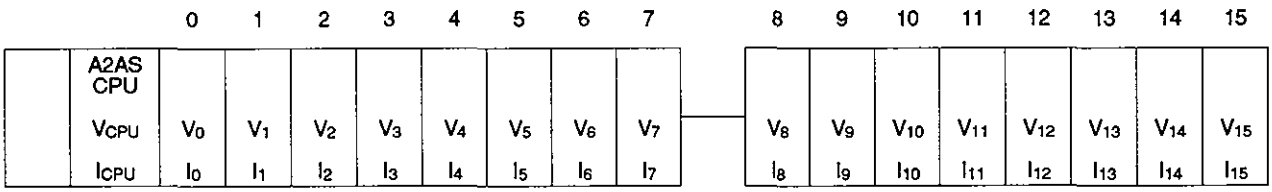
(a) Voltage drop of a main base unit

(b) Voltage drop of an extension base unit

(c) Voltage drop over an extension cable

	Extension cable connected to the left side of main base unit (serial)	Extension cable connected to the right side of main base unit (parallel)
A1S52B(S1), A1S55B(S1), or A1S58B(S1) extension base unit is used	 Voltage drop of the main base unit can be ignored.	
A55B or A58B extension base unit is used	 Voltage drop of the main and the extension base units can be ignored.	 Voltage drop of the extension base units can be ignored.

(3) Calculation of the receiving-end voltage



V_{CPU}, V_0 to V_7 : Voltage drop of each slot of a main base unit
I_{CPU}, I_0 to I_7 : Current consumption of each slot of a main base unit
V_8 to V_{15} : Voltage drop of each slot of an extension base unit
I_8 to I_{15} : Current consumption of each slot of an extension base unit

(a) Calculation of voltage drop of a main base unit (A1S32B, A1S33B, A1S35B, A1S38B)

Each slot of a main base unit has a resistance of 0.007 Ω. Calculate the voltage drop of each slot, and obtain the total voltage drop of a main base unit.

1) Voltage drop of a CPU module: V_{CPU}

$$V_{CPU} = 0.007 \times (0.4 + I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

2) Voltage drop of slot 0: V_0

$$V_0 = 0.007 \times (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

3) Voltage drop of slot 1: V_1

$$V_1 = 0.007 \times (I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

4) Voltage drop of slot 2: V_2

$$V_2 = 0.007 \times (I_2 + I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

5) Voltage drop of slot 3: V_3

$$V_3 = 0.007 \times (I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

6) Voltage drop of slot 4: V_4

$$V_4 = 0.007 \times (I_4 + I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

7) Voltage drop of slot 5: V_5

$$V_5 = 0.007 \times (I_5 + I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

8) Voltage drop of slot 6: V_6

$$V_6 = 0.007 \times (I_6 + I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

9) Voltage drop of slot 7: V_7

$$V_7 = 0.007 \times (I_7 + I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$$

10)Total voltage drop of a main base unit: V_K

$$V_K = V_{CPU} + V_0 + V_1 + V_2 + V_3 + V_4 + V_5 + V_6 + V_7$$

(b) Calculation of voltage drop of an extension base unit (A1S52B, A1S55B, A1S58B)

Each slot of an extension base unit has a resistance of 0.006 Ω. Calculate the voltage drop of each slot, and obtain the total voltage drop of an extension base unit.

1) Voltage drop of slot 8: V_8

$V_8 = 0.006 \times (I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$

2) Voltage drop of slot 9: V_9

$V_9 = 0.006 \times (I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$

3) Voltage drop of slot 10: V_{10}

$V_{10} = 0.006 \times (I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$

4) Voltage drop of slot 11: V_{11}

$V_{11} = 0.006 \times (I_{11} + I_{12} + I_{13} + I_{14} + I_{15})$

5) Voltage drop of slot 12: V_{12}

$V_{12} = 0.006 \times (I_{12} + I_{13} + I_{14} + I_{15})$

6) Voltage drop of slot 13: V_{13}

$V_{13} = 0.006 \times (I_{13} + I_{14} + I_{15})$

7) Voltage drop of slot 14: V_{14}

$V_{14} = 0.006 \times (I_{14} + I_{15})$

8) Voltage drop of slot 15: V_{15}

$V_{15} = 0.006 \times I_{15}$

9) Total voltage drop of an extension base unit: V_Z

$V_Z = V_8 + V_9 + V_{10} + V_{11} + V_{12} + V_{13} + V_{14} + V_{15}$

(c) Calculation of voltage drop over extension cables

[1] Total current consumption of an extension base unit: I_Z

$I_Z = I_8 + I_9 + I_{10} + I_{11} + I_{12} + I_{13} + I_{14} + I_{15}$

[2] Voltage drop over an extension cable: V_C

V_C = (Resistance of an extension cable) x I_Z

Resistance of extension cables

A1SC01B	0.02 Ω	A1SC30B	0.121 Ω
A1SC03B	0.021 Ω	A1SC60B	0.182 Ω
A1SC07B	0.036 Ω	A1SC05NB	0.037 Ω
A1SC12B	0.055 Ω	A1SC07NB	0.045 Ω

(d) Voltage at the receiving end

(5.1 (V) - VK - VZ - VC) ≥ 4.75 (V)

POINT

If 3 extension base units are installed, determine the voltage at the receiving end as follows:

(1) Calculation of voltage drop at the main base unit

Determine the voltage drop at individual slots by multiplying the resistance of one slot (0.007 Ω) by the [sum of current consumptions of all slots in the main base unit + sum of current consumptions of all slots in the 1st, 2nd and 3rd extension base units], then sum the voltage drops at the individual slots.

(2) Calculation of voltage drop at 1st extension base unit

Determine the voltage drop at individual slots by multiplying the resistance of one slot (0.006 Ω) by the [sum of current consumptions of all slots in the 1st extension base unit + sum of current consumptions of all slots in the 2nd and 3rd extension base units], then sum the voltage drops at the individual slots.

(3) Calculation of voltage drop at 2nd extension base unit

Determine the voltage drop at individual slots by multiplying the resistance of one slot (0.006 Ω) by the [sum of current consumptions of all slots in the 2nd extension base unit + sum of current consumptions of all slots in the 3rd extension base unit], then sum the voltage drops at the individual slots.

(4) Calculation of voltage drop at 3rd extension base unit

Determine the voltage drop at individual slots by multiplying the resistance of one slot (0.006 Ω) by the [sum of current consumptions of all slots in the 3rd extension base unit], then sum the voltage drops at the individual slots.

(5) Calculation of voltage drop in the extension cable

Calculate the sum of (a) + (b) + (c):

(a) (Resistance of the extension cable that connects the main base unit and 1st extension base unit) x (sum of current consumptions of 1st, 2nd and 3rd extension base units)

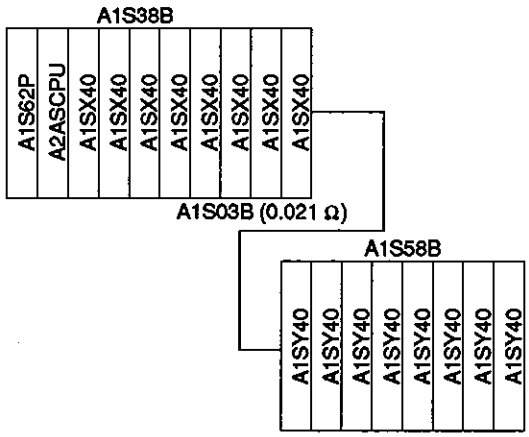
(b) (Resistance of the extension cable that connects the 1st extension base unit and 2nd extension base unit) x (sum of current consumptions of 2nd and 3rd extension base units)

(c) (Resistance of the extension cable that connects the 2nd extension base unit and 3rd extension base unit) x (total current consumption of 3rd extension base unit)

(6) Checking the voltage at the receiving end

5.1 - (sum of (1) through (5)) ≥ 4.75 (V)

(4) Examples



(a) Calculation of voltage drop of a main base unit

VK = 0.007 x {0.4 + 0.05 x (8 + 7 + 6 + 5 + 4 + 3 + 2 + 1) + (0.27 x 8) x 8} = 0.13636

(b) Calculation of voltage drop of an extension base unit

VZ = 0.006 x 0.27 x (8 + 7 + 6 + 5 + 4 + 3 + 2 + 1) = 0.05832

(c) Calculation of voltage drop over an extension cable

VC = 0.036 x (0.27 x 8) = 0.07776

(d) Voltage at the receiving end

5.1 - 0.13636 - 0.05832 - 0.07776 = 4.82756(V)

Since the voltage at the receiving end is more than 4.75V, the above system can be put into operation.

(5) Minimizing the voltage drop

Try the following to minimize the voltage drop:

(a) Change the positions of modules.

Install the modules in a main base unit from slot 0 in the descending order of current consumption. Install the modules of small current consumption in extension base units.

(b) Connect the base units in series.

By connecting the base units in series (connecting an extension cable to the left side of a main base unit), the voltage drop of the main base unit can be minimized. But when a long extension cable is used for this connection, the extension cable may cause a larger voltage drop than that of the main base unit. In such a case, calculate the voltage drop as mentioned in (3).

(c) Use a short extension cable.

The shorter the extension cable, the smaller the resistance it has, consequently minimizing its voltage drop. Use as short extension cables as possible.

6.2 Handling

This section gives base unit handling instructions, notes on using the extension bases, nomenclature and hardware setting instructions.

6.2.1 Handling instructions

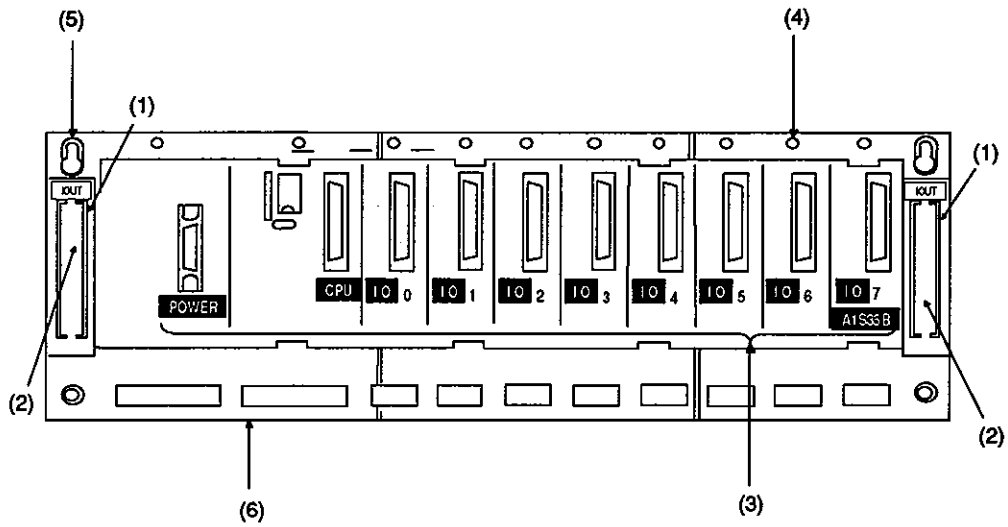
(1) Do not subject the base unit to impact or shock.

(2) Do not remove printed circuit boards form the housing. There are no user-serviced parts on the boards.

(3) Ensure that no conductive debris can enter the module. If it does, make sure that it is removed. Guard particularly against wire offcuts.

6.2.2 Nomenclature and settings

(1) Main base unit (A1S32B, A1S35B, A1S38B)



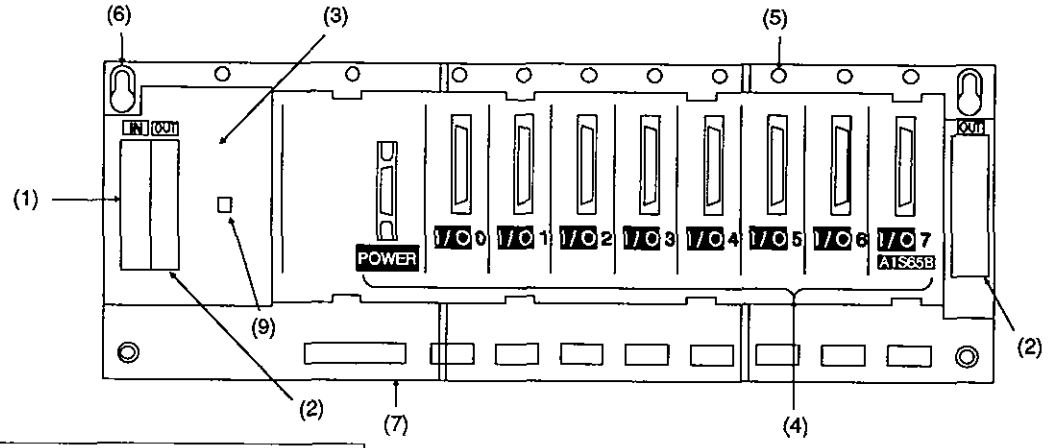
No.	Name	Application
(1)	Connector for extension cable	Connector for sending and receiving signals to and from the extension base unit. (The A1S32B is not provided with connectors)
(2)	Base cover	Cover for protection of connector for extension cable. When connecting an extension cable, remove the appropriate base cover located below the word "OUT" with nippers or a similar tool.
(3)	Module connectors	Connectors where the power supply module, CPU module, I/O module, special-function modules are loaded. Load the connector cover or blank cover (A1SG60) to vacant connectors, in order to protect the module from dust.
(4)	Module fixing screw	Screw to fix a module to the base unit. Screw size: M4 x 12 screw
(5)	Guide hole for base installation	Slot for mounting this base unit to the panel of control box, etc. (For M5 screw)
(6)	DIN rail hook	Hook to install DIN rail. A1S32B, A1S33B.....1 A1S35B, A1S38B.....2

IMPORTANT

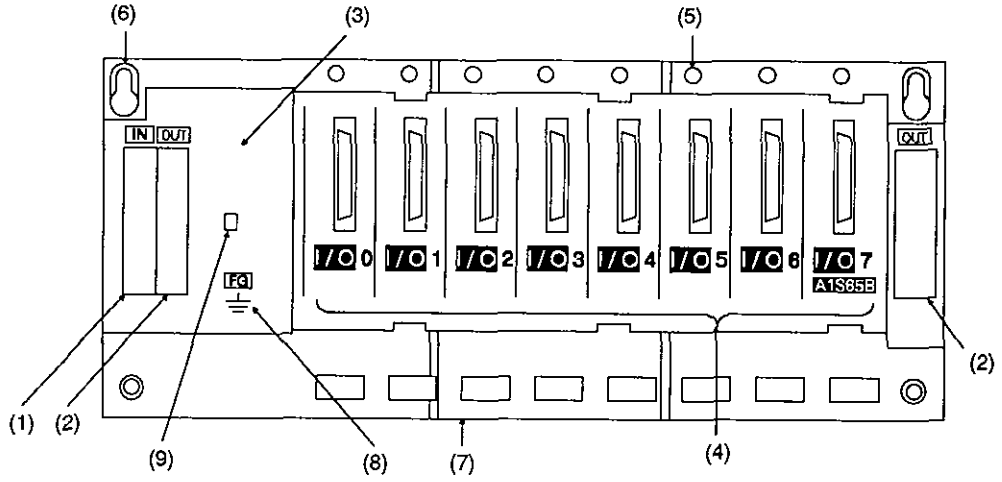
Only one single extension base unit can be loaded to the main base unit. Loading two extension base units to the extension connectors of the main base unit could cause an I/O error.

(2) Extension base units

A1S65B(S1), A1S68B(S1)



A1S52B(S1), A1S55B(S1), A1S58B(S1)



No.	Name	Purpose
(1)	Extension cable connector (IN)	Used to connect an extension cable to an extension base unit or a main base unit for signal transmissions. Remove the connector cover attached to the unit and connect an extension cable.
(2)	Extension cable connector (OUT) (for A1S[ ][ ]B-S1)	
(3)	Base cover	Extension cable connector protective cover.
(4)	Module connector	Used to connect to power supply module, an I/O module or special function module. Put a supplied cover or blank cover (A1SG60) on unused connector to protect it from dust.
(5)	Module mounting screw	Used to secure a module to the base unit. Screw size: M4 x 12
(6)	Base mounting hole	Used to mount the base unit to a control panel. (for M5 screw)
(7)	DIN rail hook	Used to install the module to the DIN rail. A1S52B(S1), A1S55B(S1): One hook A1S65B(S1), A1S68B(S1), A1S58B(S1): Two hooks
(8)	FG terminal	Grounding terminal connected to the shield pattern on the PC board.
(9)	Stage number setting switch (for A1S[ ][ ]B-S1)	Switch for setting the stage number of extension base. For the stage number setting procedure, refer to Section 6.3.

6.2.3 Installing a DIN rail

Both the main base units and extension base units are equipped with hooks used for mounting to a DIN rail.

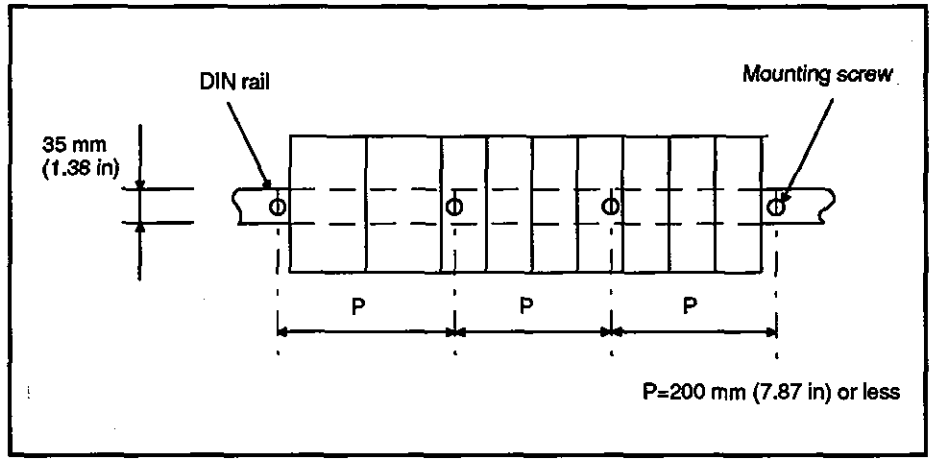
The following explains the method of mounting a DIN rail:

(1) Applicable DIN rails (JIS-C2B12)

TH35-7.5 Fe
TH35-7.5 Al
TH35-15 Fe

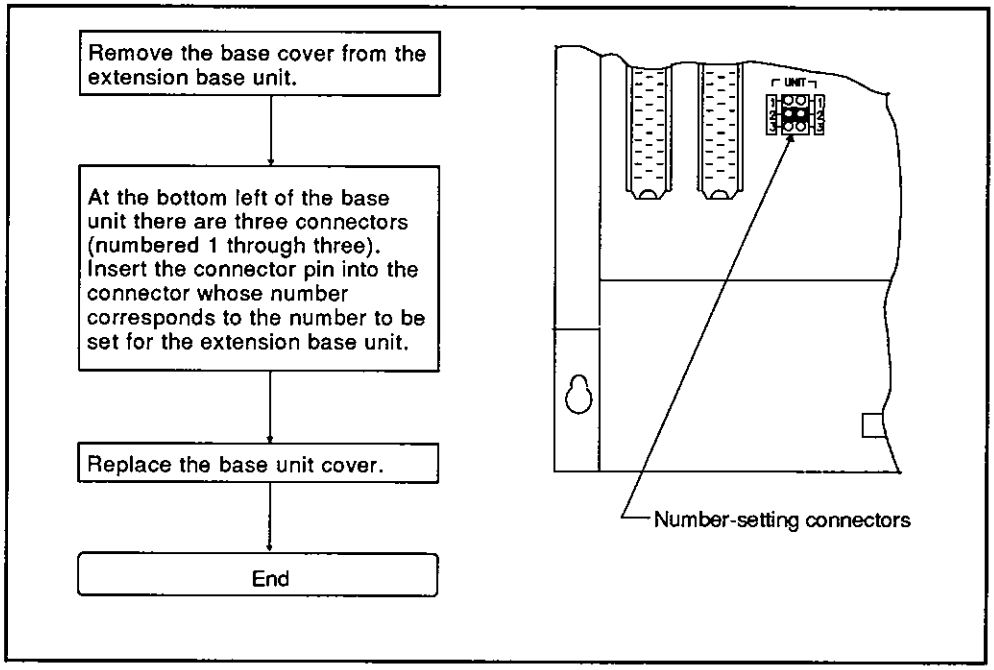
(2) Intervals of mounting screws

When a TH35-7.5 Fe or TH35-7.5 Al rail is mounted, fix it with screws with intervals of 200 mm or less between each of the screws.



6.3 Extension Base Number Setting (A1S[ ][ ]B-S1 Extension Base Units Only)

This section describes the method for setting the extension base unit numbers when extension base units are used.



Extension base unit number setting

	Setting		
	1st	2nd	3rd
Setting of number-setting connectors	UNIT 1 2 3	UNIT 1 2 3	UNIT 1 2 3

POINT

Set one of the connectors, 1 through 3, whose number corresponds to the number to be set for the extension base unit. Do not set more than one connector, set the same connector number at more than one unit, or fail to set any connector number, since erroneous inputs and outputs will result.

7. MEMORY ICs AND BATTERY

7.1 Memory ICs

This section describes specifications, handling instructions and installation of the memory ICs used in the A2ASCPU.

7.1.1 Specifications

Table 7.1 shows specifications of the ROMs.

Table 7.1 Memory Specifications

Item \ Model	A2SMCA-14KE	A2SMCA-14KP
Memory specifications	EEP-ROM	EP-ROM
Memory capacity (bytes)	64K bytes (max. 14 K steps)	
Outside dimension mm (in)	15 x 68.6 x 42 (0.59 x 2.7 x 1.65)	
Weight (kg) (lb)	0.03 (0.06)	

7.1.2 Handling instructions

(1) Handle with care memory cassettes and pin connectors since their plastic body cannot resist strong impacts.

(2) Do not remove the printed circuit board from the memory cassette.

(3) Use caution not to let chips of wires and other foreign material enter the memory cassette.

(4) When installing a memory cassette to an A2ASCPU module, engage the connectors securely.

(5) Never place the memory on metal, which may allow current flow, or on an object which is charged with static electricity, such as wood, plastic vinyl, fiber, cable and paper.

(6) Do not touch or bend the memory leads.

(7) Do not touch by hand the connector of a memory cassette. Touching it by hand may lead to incomplete contact.

IMPORTANT

(1) Always turn OFF the power to the A2ASCPU module when installing or removing a memory cassette. If a memory cassette is installed or removed with the power to the CPU ON, contents of the memory will be destroyed.

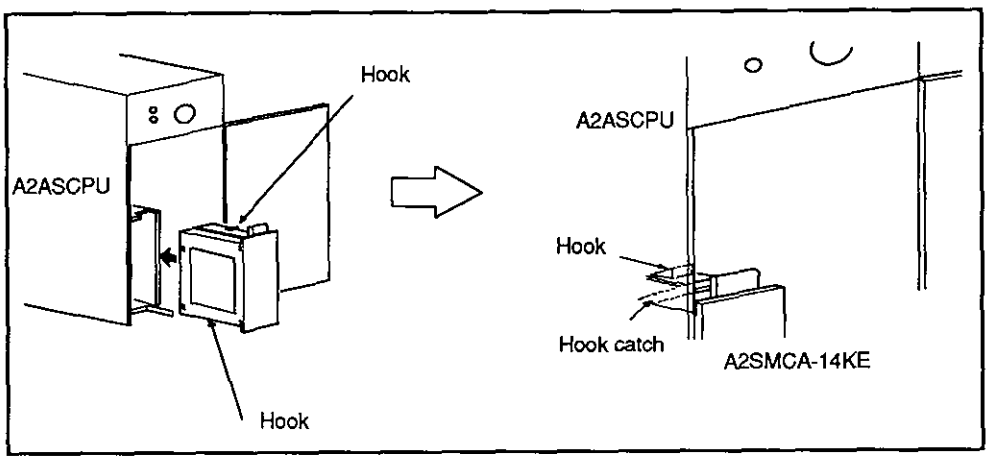
(2) If the power is turned ON when the memory cassete is installed, the contents of the RAM memory incorporated in the A2ASCPU is over-written.
If the contents of the RAM memory needs to be saved, install a memory cassette after making a backup of the contents using a peripheral device.

(3) The A1SMCA-[ ]KE/[ ]KP memory cassette cannot be used for A2ASCPU.

7.1.3 Installing and removing a memory cassette

Follow the procedures below when installing or removing a memory cassette.

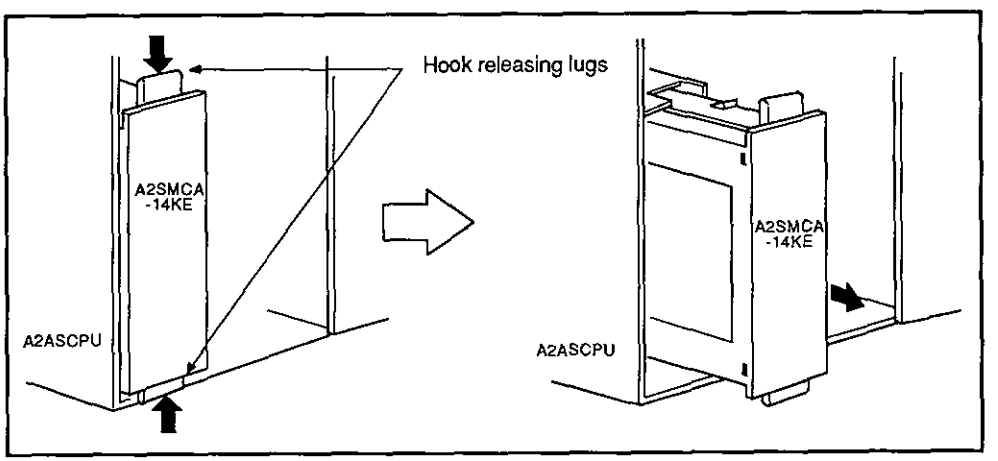
(1) Installing a memory cassette



(a) Hold a memory cassette vertically so that its model name is right side up and its connector faces the A2ASCPU module. Insert the memory cassette all the way in the A2ASCPU module so that the hooks of the memory cassette are completely engaged (they "click").

(b) Make sure the hooks are completely engaged. (If the memory cassette is not inserted all the way, the front lid of the A2ASCPU cannot be closed.)

(2) Removing a memory cassette



(a) Pull out the memory cassette while pushing the hook releasing lugs that are provided at the top and the bottom of the memory cassette.

7.1.4 Writing a sequence program to an A2SMCA-14KP

A sequence program can be written to, or erased from, an A2SMCA-14KP using a ROM writer/eraser.

If an A2SMCA-14KP is installed to the ROM socket of an A6GPP or A6WU, use a memory write adaptor (A2SWA-28P).

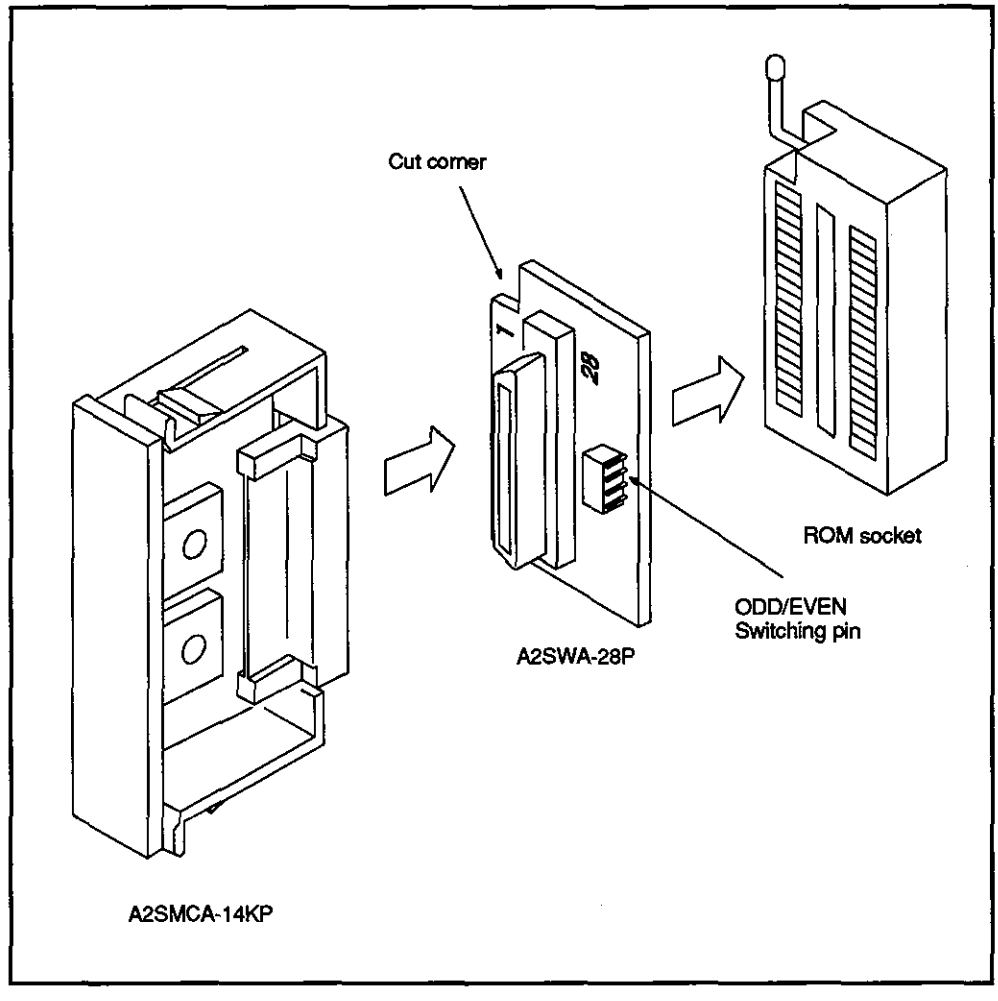
Use an A2SWA-28P as follows:

(1) The program must be written only to either of even- or odd-numbered addresses of an A2SMCA-14KP.
Set the type of the addresses using the ODD/EVEN setting selector pin of the A2SWA-28P.

(2) Install an A2SMCA-14KP to an A2SWA-28P so that their connectors couple correctly with each other.

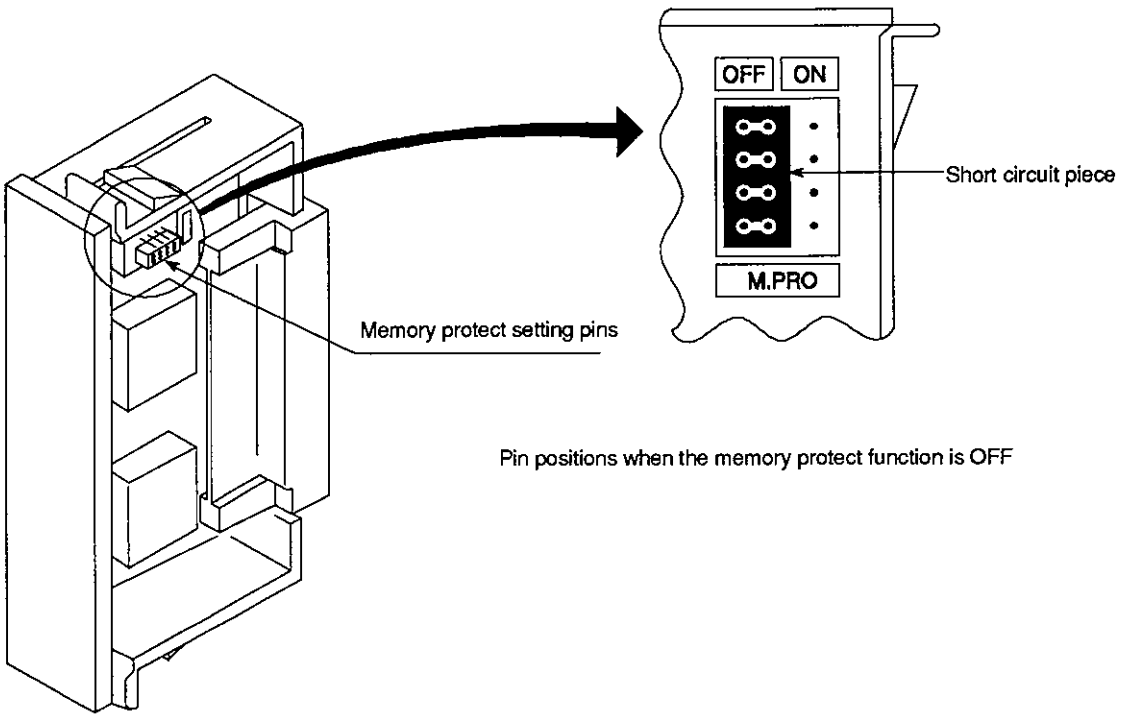
(3) Install the A2SWA-28P that is coupled with an A2SMCA-14KP to the ROM socket of an A6GPP or A6WU.

The pin next to the cut corner of the A2SWA-28P is pin No. 1. Make sure the A2SWA-28P is installed correctly to the ROM socket.



7.1.5 A2SMCA-14KE memory protect setting

To protect the data stored in ROM memory from being overwritten by accidental incorrect operation of peripheral devices when an A2SMCA-14KE is attached to the A2ASCPU, memory protect setting can be made on the A2SMCA-14KE.
Turning ON the memory protect setting pins can batch-protect the 64-Kbyte user memory area.
When changing the data in ROM memory, turn OFF the memory protect setting pins.
The memory protect setting pins are all set to OFF when delivered.
For allocation of memory areas, see Section 4.4.2.



Pin positions when the memory protect function is OFF

A2SMCA-14KE

7.2 Battery

7.2.1 Specifications

Table 7.2 shows specifications of the battery used to retain memory stored if power failure occurs.

Table 7.2 Battery Specifications

Item \ Model	A6BAT
Normal voltage	3.6 VDC
Guaranteed life	5 years
Application	For IC-RAM memory backup and power failure compensation function
External dimension mm(in)	ϕ16(0.63)×30(1.18)

7.2.2 Handling instructions

(1) Do not short circuit.

(2) Do not disassemble.

(3) Do not expose to open flame.

(4) Do not heat.

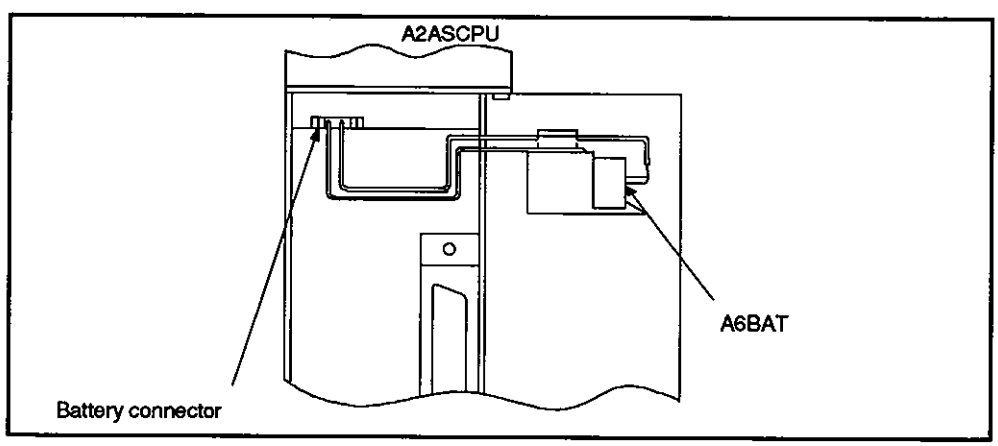
(5) Do not solder its terminals.

7.2.3 Installation

Battery lead connector is disconnected from the battery connector on the A2ASCPU board to prevent discharge during transportation and storage.

Before starting the A2ASCPU, plug the battery connector into the battery connector on the A2ASCPU board.

- To use a sequence program stored in the user program area in the A2ASCPU if a power failure occurs.
- To retain the data if a power failure occurs.



8. LOADING AND INSTALLATION

8.1 Consideration for Safety

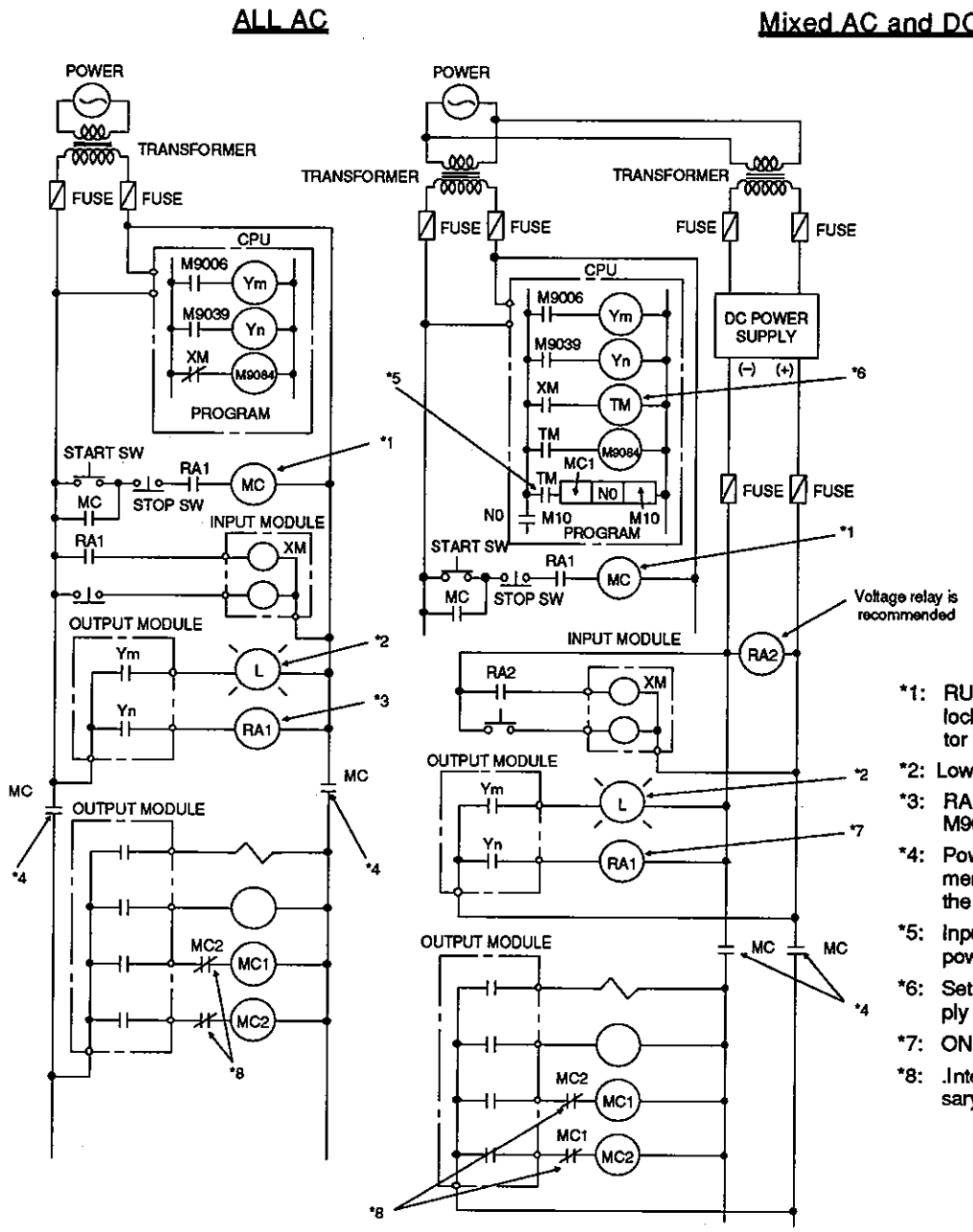
When the power to the system is turned ON or OFF, the process output may not perform normally at times due to the difference between the delay time and the rise time of the power supply of the PC CPU main module and the external power supply (especially DC). Also, if there is an error in the external power supply, the output process may malfunction.

To (a) prevent erroneous operation of the entire system, and (b) ensure safety, prepare circuits (such as an emergency stop circuit, protection circuit, and interlock circuit) that prevent machine damage and/or accidents due to erroneous operation of peripheral devices. A sample system design circuit based on this concept is given on the following page.

POINT

Some types of the A1S series output module detect a blown fuse error as soon as the external power supply is turned ON.
In the sample circuit illustrated on the next page, since the start-up of the A2ASCPU takes place earlier than the rise of the external power supply to the output module, a blown fuse error is detected.
To solve this problem, the system is designed to keep the M9084 ON until the external power supply rises so as not to check blown fuses.
(When the M9084 is ON, I/O module comparison and battery checks are not performed.)

(1) System design circuit example



*1: RUN/STOP circuit interlocked with RA1 (run monitor relay)

*2: Low battery alarm

*3: RA1 switched ON by M9039 (run monitor relay)

*4: Power to output equipment switched OFF when the STOP signal is given.

*5: Input switched when power supply established.

*6: Set time for DC power supply to be established.

*7: ON when run by M9039

*8: .Interlock circuits as necessary.

The power-ON procedure is as follows:

For AC

1) Switch ON the power.
2) Set the CPU to RUN.
3) Turn ON the start switch.
4) When the magnetic contactor (MC) comes in, the output equipment is powered and may be driven by the program.

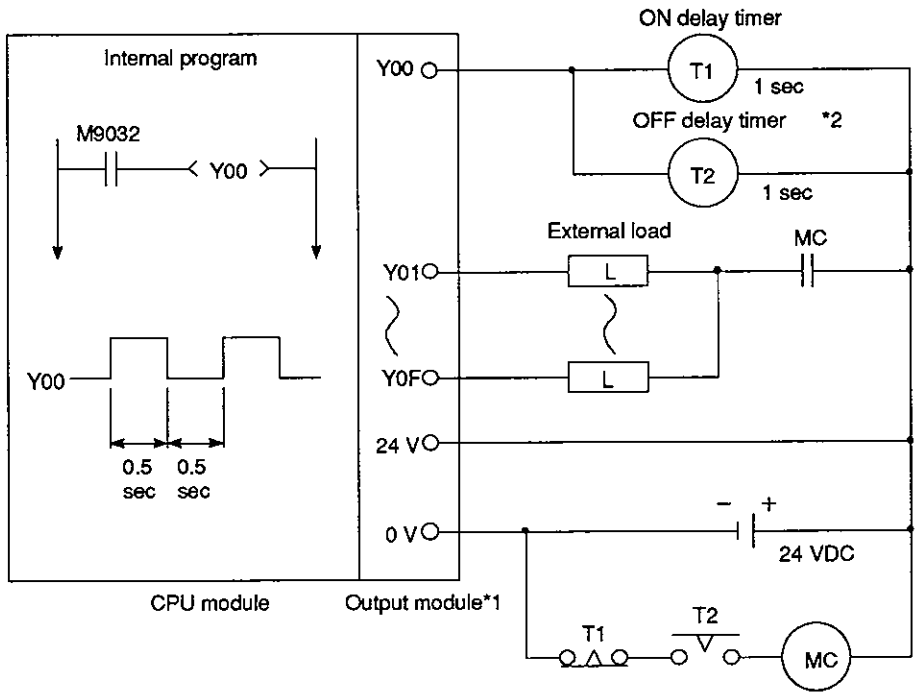
For AC/DC

1) Switch ON the power.
2) Set the CPU to RUN.
3) When DC power is established, RA2 goes ON.
4) Timer (TM) times out after the DC power reaches 100%.

   (The TM set value should be the period of time from when RA2 goes ON to the establishment of 100% DC voltage. Set this value to approximately 0.5 seconds.)
5) Turn ON the start switch.
6) When the magnetic contractor (MC) comes in, the output equipment is powered and may be driven by the program.

(2) Fail-safe measures against PC failures

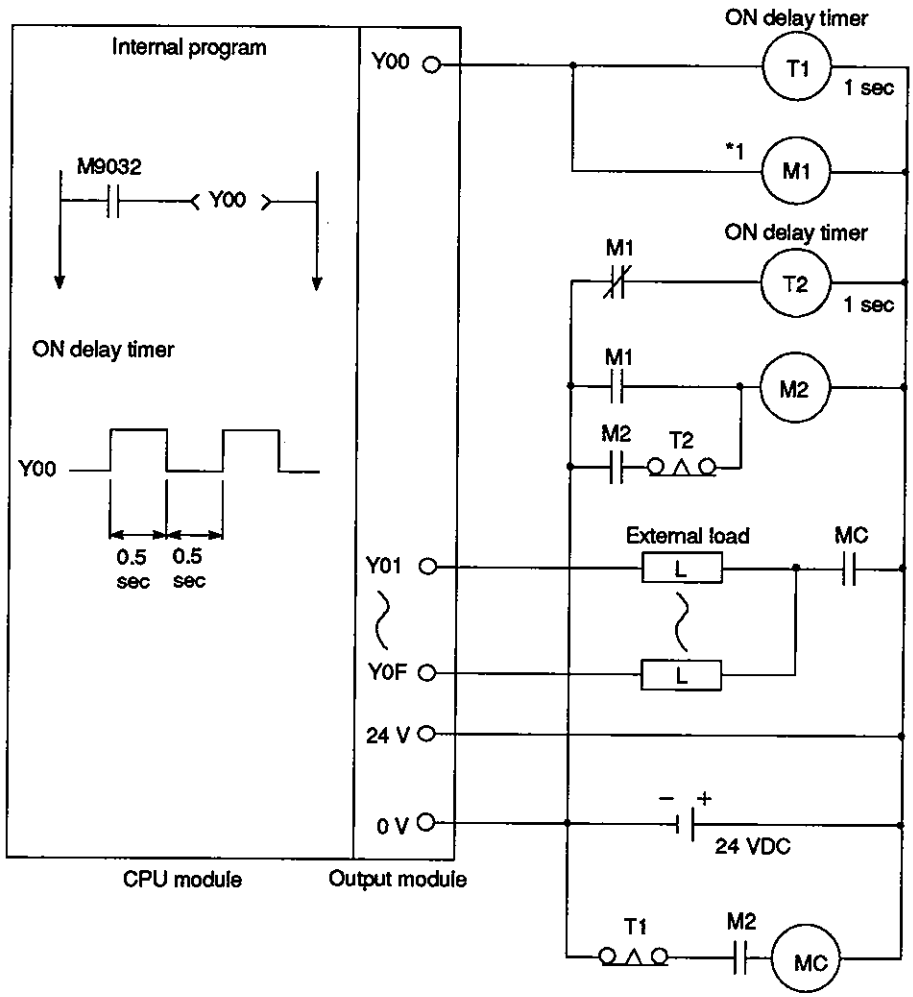
Problems with the CPU or memory can be detected by the self diagnosis function. However, problems with the I/O control area may not be detected by the CPU.
In such cases, all I/O points turn ON or OFF depending on the condition of problem, and normal operating conditions and operating safety cannot sometimes be maintained.
Though Mitsubishi PCs are manufactured under strict quality control, they may cause failure or abnormal operations due to unspecific reasons. To prevent the abnormal operation of the whole system, machine breakdown, and accidents, build a fail-safe circuit outside the PC.
The following gives an example of a fail-safe circuitry.



*1: Y00 repeats turning ON and then OFF at 0.5 second intervals. Use a no-contact output module (transistor in the example shown above).

*2: If an OFF delay timer (especially a miniature timer) is not available, use ON delay timers to make a fail-safe circuit as shown on the next page.

A fail-safe circuit built with ON delay timers



*1: Use a solid-state relay for the M1 relay.

8.2 Installation Environment

Never install the A2ASCPU system in the following environments:

(1) Locations where the ambient temperature is outside the range of 0 to 55°C.

(2) Locations where the ambient humidity is outside the range of 10 to 90% RH.

(3) Locations where dew condensation takes place due to sudden temperature changes.

(4) Locations where there are corrosive and/or combustible gasses.

(5) Locations where there is a high level of conductive powder (such as dust and iron filings, oil mist, salt, and organic solvents).

(6) Locations exposed to the direct rays of the sun.

(7) Locations where strong power and magnetic fields are generated.

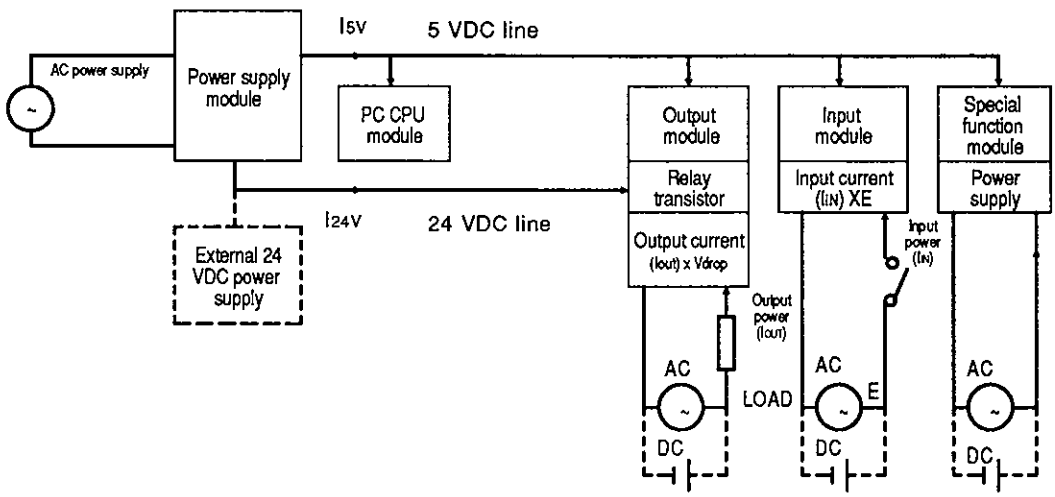
(8) Locations where vibration and shock are directly transmitted to the main module.

8.3 Calculation of Heat Generated by the Programmable Controller System

The operating ambient temperature of the PC must be kept below 55°C. The heat generated by the PC should be dissipated by fans or similar equipment. It is calculated as follows:

Average power consumption

Power is consumed by the following PC areas:



(1) Power consumption of a power supply module

Approximately 70% of the power supply module current is converted into power and 30% of that 70% is dissipated as heat, i.e., 3/7 of the output power is actually used.

$$Wpw = \frac{3}{7} \{(I_{5V} \times 5) + (I_{24V} \times 24)\} (W)$$

where, I_{5V} = VDC logic circuit current consumption of each module.
I_{24V} = current consumption of the output modules (with an average number of points switched ON) ...(Not for 24 VDC input power supply modules)

(2) Total 5 VDC power consumption

5 VDC is supplied to each module via the base plate, which powers the logic circuitry.

$W_{5V} = I_{5V} + 5(W)$

(3) Total 24 VDC output module power consumption (with an average number of points switched ON)

24 VDC is supplied to drive output devices.

$W_{24V} = I_{24V} \times 24 (W)$

(4) Power consumption of output circuits (with an average number of points switched ON)

$W_{OUT} = I_{OUT} \times$ Vdrop x average number of outputs on at one time (W)

where, I_{OUT} =output current (actual operating current) (A)
Vdrop =voltage dropped across each output load (V)

(5) Power consumption of input circuits (with an average number of points switched ON)

$W_{IN} = I_{IN} \times E \times$ average number of inputs on at one time (W)

Where, I_{IN} = input current (effective value for AC) (A)
E = input voltage (actual operating voltage) (V)

(6) Power consumption of the special function module power supply is expressed as:

$W_S = I_{5V} \times 5 + I_{24V} \times 24 + I_{100V} \times 100$ (W)

The sum of the above values is the power consumption of the entire PC system.

$W = W_{PW} + W_{5V} + W_{24V} + W_{OUT} + W_{IN} + W_S$ (W)

Further calculations are necessary to work out the power dissipated by the other equipment in the panel.

Generally, the temperature rise in the panel is expressed as:

$T = \frac{W}{UA}$ (°C)

where, W = power consumption of the entire PC system (obtained as shown above)

A = panel inside surface area (m^2)

U = 6 (if the panel temperature is controlled by a fan, etc.)

4 (if panel air is not circulated)

POINT

Fans, heat exchangers, or cooling units must be installed if the panel temperature is expected to exceed 55°C.

Fans should be fitted with surface filters and guards.

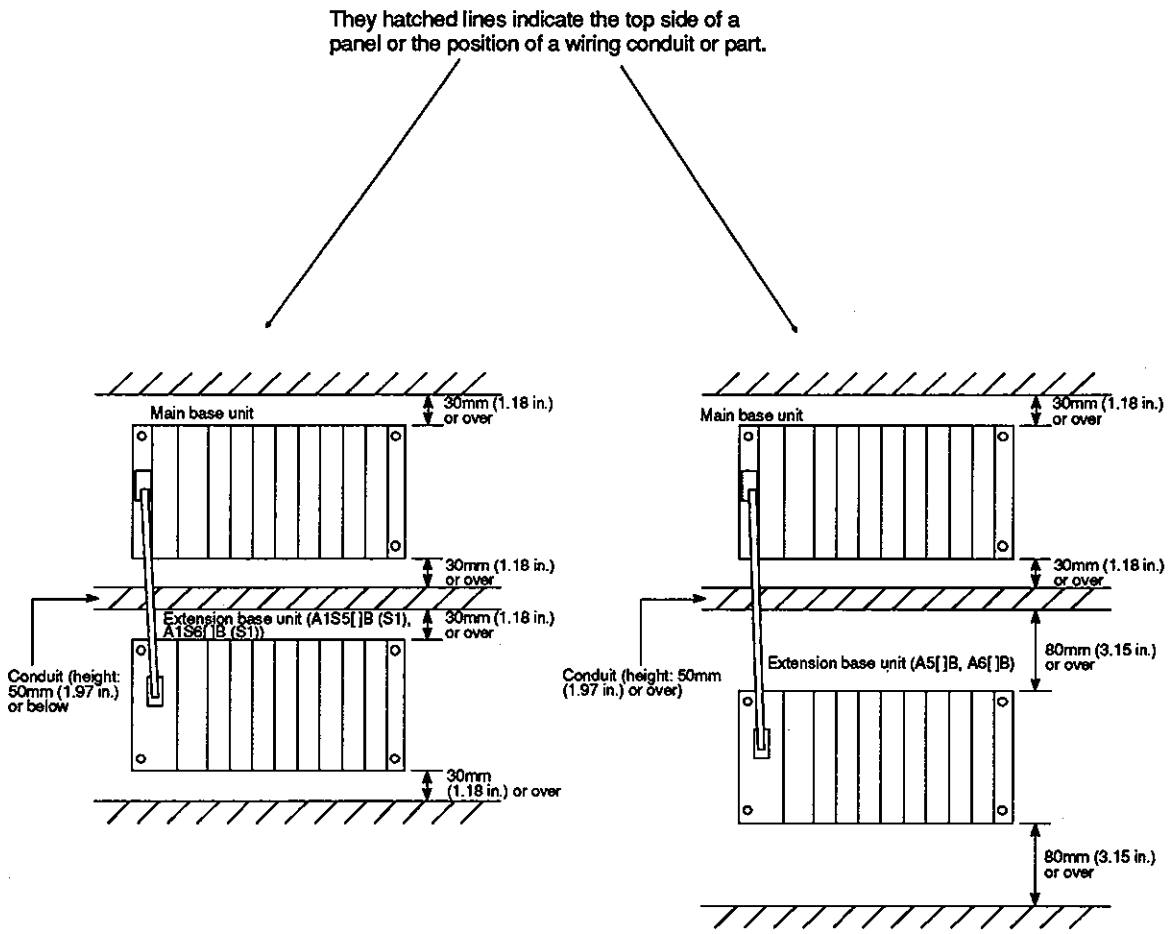
8.4 Cautions for Installing a Base Unit

Mount a PC on a panel with due consideration for operability, maintainability and environmental resistance.

(1) Base unit mounting position

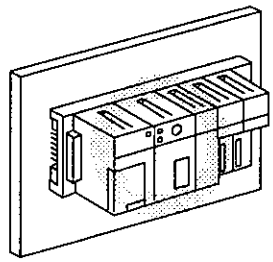
To keep the unit cool and make unit replacement easy, allow the specified clearances between the unit and the surrounding devices or parts, as shown below.

- A1S3[ ]B, A1S5[ ]B (S1), A1S6[ ]B (S1) ..... 30mm (1.18 in.) or over
- A5[ ]B, A6[ ]B ..... 80mm (3.15 in.) or over

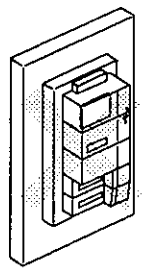


(2) Base unit mounting direction

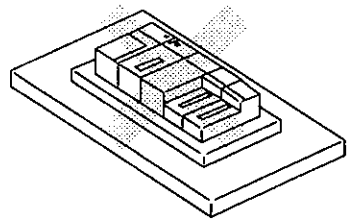
(a) Mount the PC in the direction as shown below to radiate heat.



(b) Do not mount the PC in a vertical or horizontal position.



Vertical position



Horizontal position

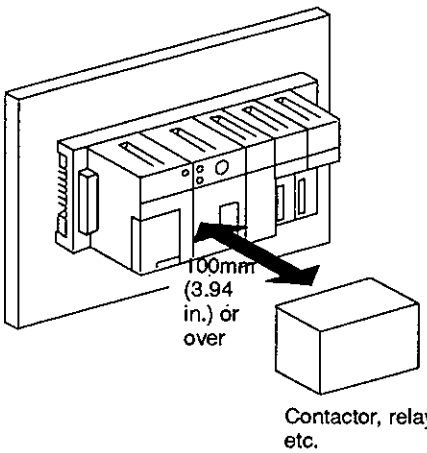
(3) Mount the base unit on a flat face.

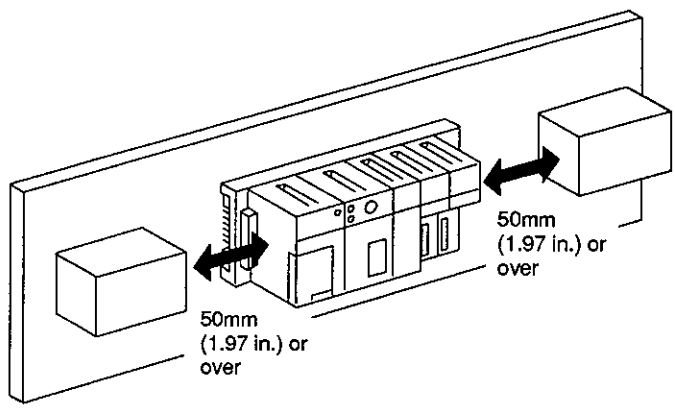
If the mounting face is uneven, an excess force may be applied to the printed circuit board, causing malfunction.

(4) Do not mount the base unit together with a large-sized electromagnetic contactor or no-fuse breaker, which produces vibration, on the same panel. Mount them on different panels, or keep the base unit away from such a vibration source.

(5) To protect the PC from radiating noise or heat, allow clearances between it and parts (contactor, relay, etc.), as shown below:

- Part mounted in front of the PC ..... 100mm (3.94 in.) or over
- Part mounted on the right or left of the PC ..... 50mm (1.97 in.) or over



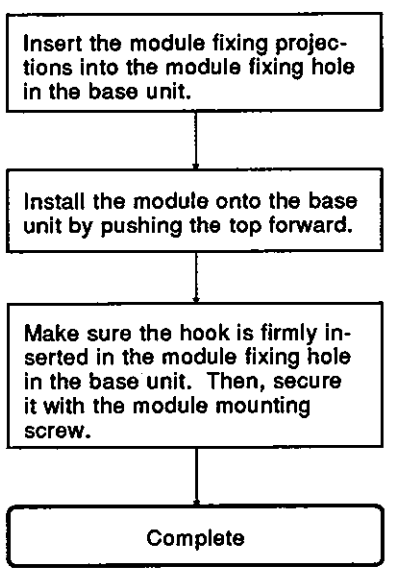


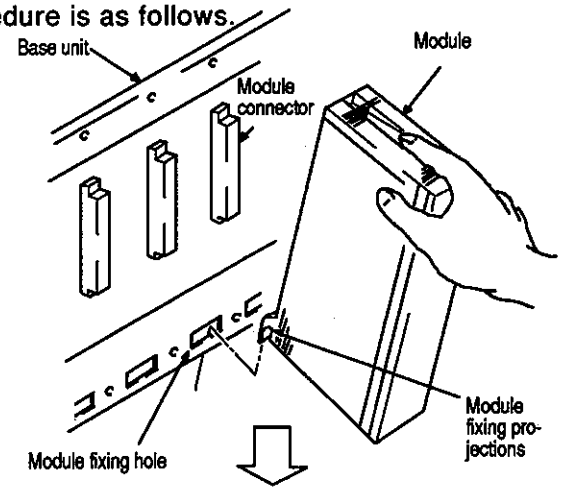
8.5 Installation and Removal of Module

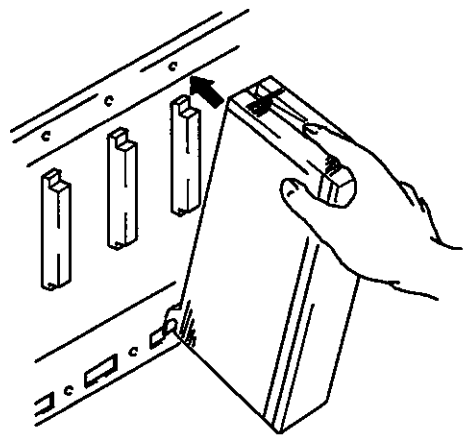
This section explains the mounting and dismounting of a power supply module, PC CPU module, I/O module, special-function module, etc. to and from the base unit.

(1) Module mounting

The module mounting procedure is as follows.



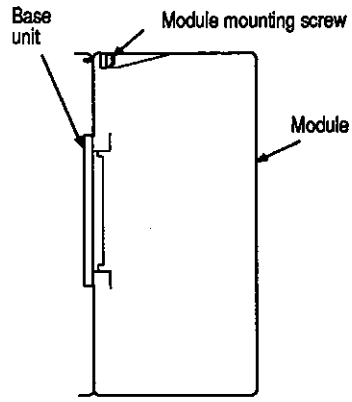




POINTS

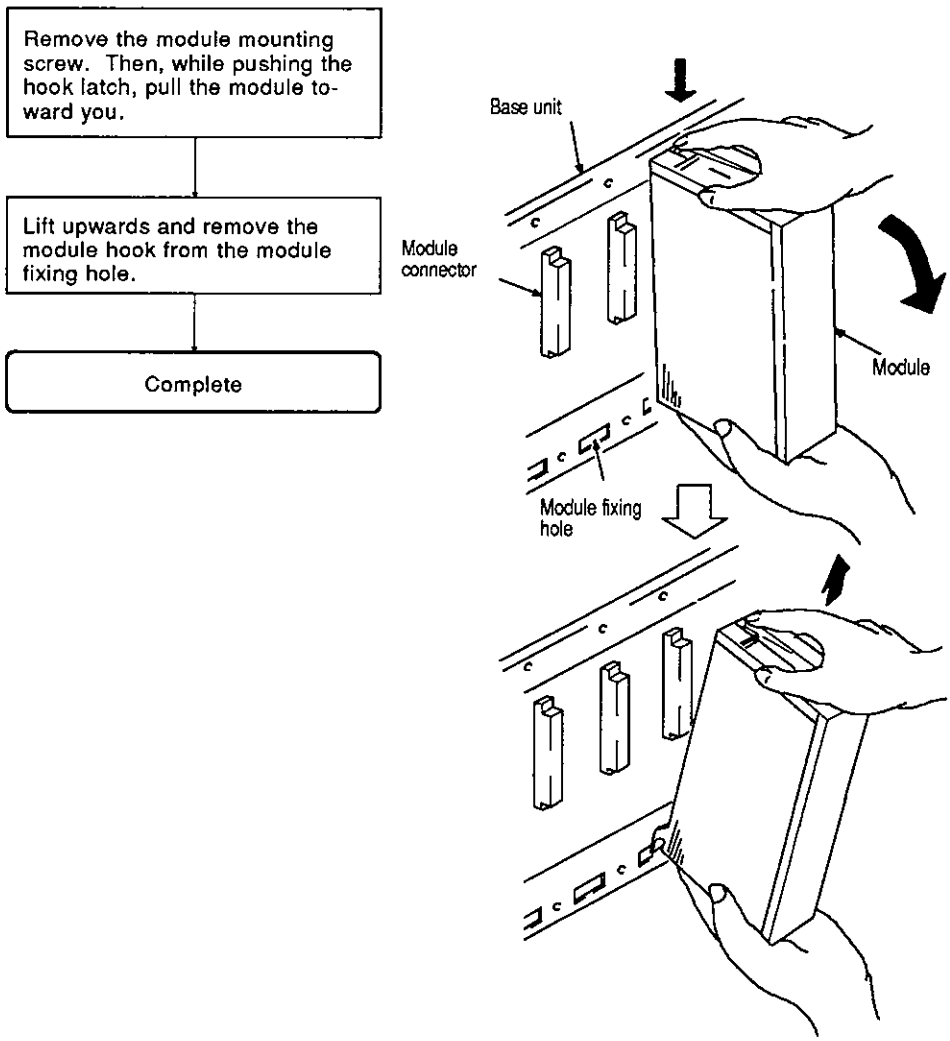
(1) To secure the module, be sure to insert the module fixing projection into the module fixing hole. If the module is forcibly secured without insertion, the pins in the module connector may be bent or damaged.

(2) Always turn the power supply OFF before mounting or dismounting any module.



(2) Module dismounting

The module dismounting procedure is as follows.



POINTS

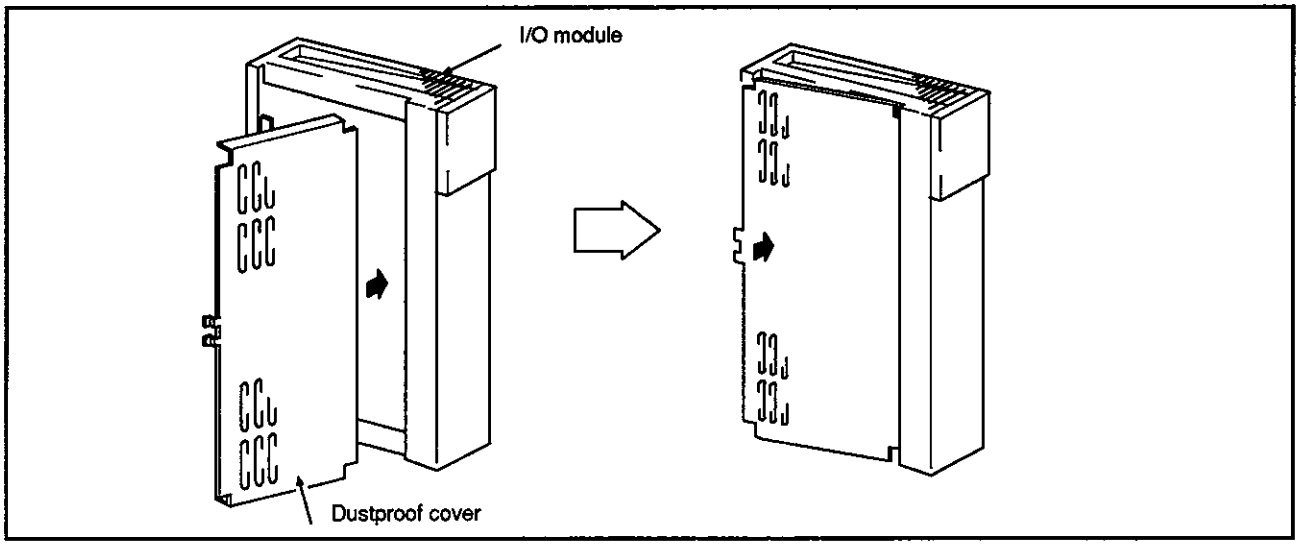
(1) To dismount the module, be sure to disengage the hook from the module fixing hole and then remove the module fixing projection from the module fixing hole. If the module is forcibly removed, the hook or module fixing projection will be damaged.

(2) Always turn the power supply OFF before mounting or dismounting.

8.6 Installing and Removing the Dustproof Cover

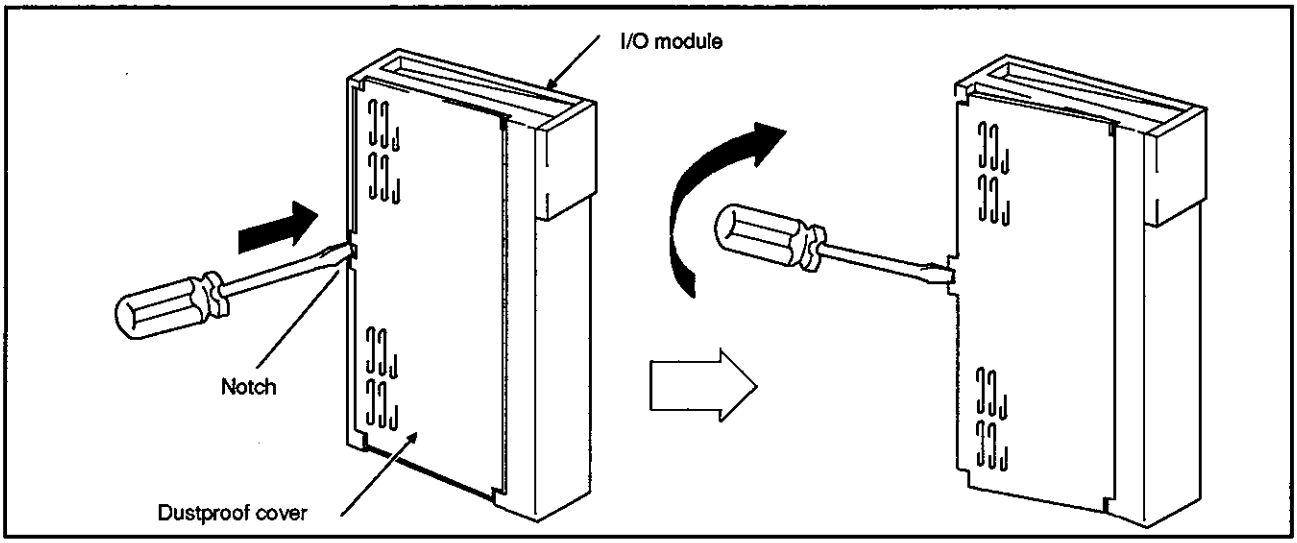
When an A1S52B(S1), A1S55B(S1), or A1S58B(S1) is used, it is necessary to install the dustproof cover, which is supplied with the base, to the I/O module loaded at the ieft end to prevent foreign matter from entering the I/O module. If the dustproof cover is not mounted, foreign matter will enter the I/O module, resulting in malfunctions. The following explains the installation and removal of the dustproof cover.

(1) Installation



To insert the dustproof cover into the I/O module, first insert the cover to the terminal side and then press the dustproof cover against the I/O module as shown in the figure.

(2) Removal



Fit the tip of a (–) head screwdriver in the notch on the left side of the dustproof cover. While keeping the screwdriver tip in the notch, gently move the screwdriver to the left (as shown above) until the cover snaps open.

8.7 Wiring

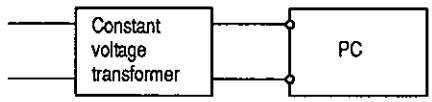
This section explains the wiring instructions for use of the system.

8.7.1 Wiring instructions

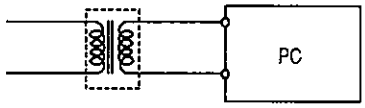
Instructions for wiring the power cable or I/O cables.

(1) Wiring of power supply

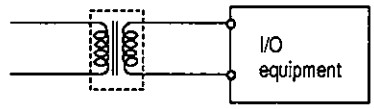
(a) When voltage fluctuations are larger than the specified value, connect a constant-voltage transformer.



(b) Use a power supply which generates minimal noise across wire and across PC and ground. When excessive noise is generated, connect an insulating transformer.



Insulating transformer



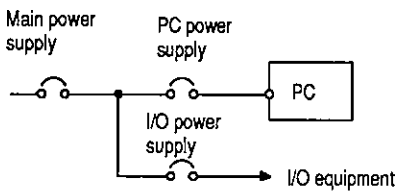
Insulating transformer

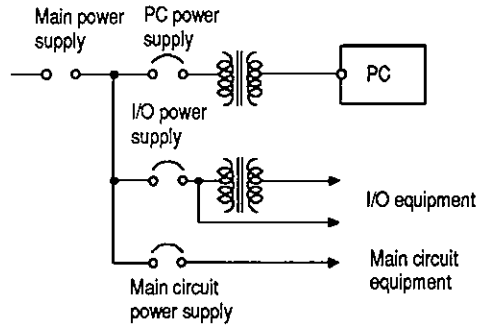
(c) When a power transformer or insulating transformer is employed to reduce the voltage from 200 VAC to 100 VAC, use one with a capacity greater than those indicated in the following table.

Power Supply Module	Transformer Capacity
A1S61P	110VA x n
A1S62P	110VA x n

"n" stands for the number of power supply modules.

(d) When wiring, separate the PC power supply from the I/O and power equipment as shown below.

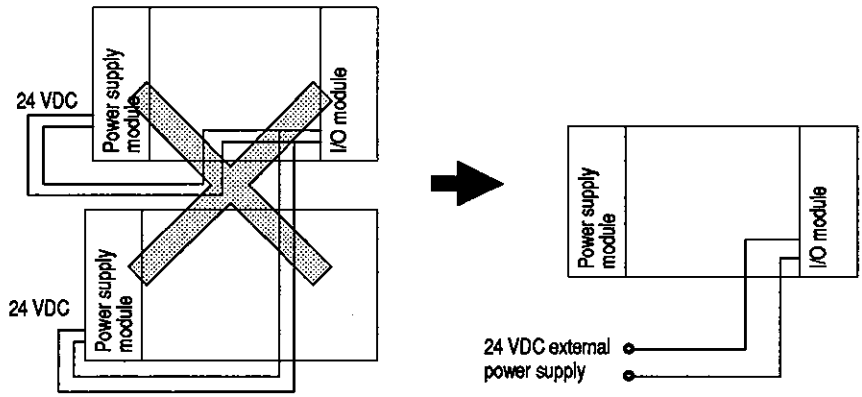




(e) Note on using 24 VDC output of the A1S62P power supply module.

To protect the power supply modules, do not supply one I/O module with 24 VDC from several power supply modules connected in parallel.

If 24 VDC output capacity is sufficient for one power supply module, supply 24 VDC from the external 24 VDC power supply as shown below:

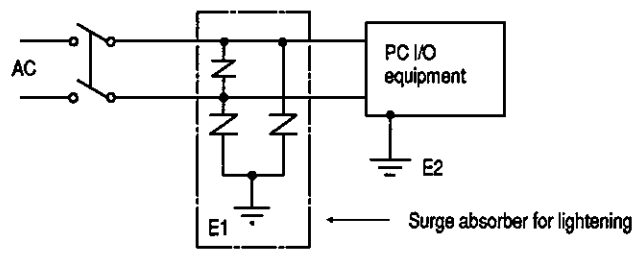


(f) Twist the 100 VAC, 200 VAC, and 24 VDC cables as closely as possible. Connect modules with the shortest possible wire lengths.

(g) To minimize voltage drop, use the thickest (max. 2 mm^2 (14 AWG)) wires possible for the 100VAC. 200 VAC, and 24 VDC cables.

(h) Do not bundle the 100 VAC and 24 VDC cables with main-circuit wires or the I/O signal wires (high-voltage, large-current). Also, do not wire the above-indicated cables close to the aforementioned wires. If possible, provide more than 100 mm (3.94 in.) distance between the cables and wires.

(i) As a lightning-protection measure, connect a surge absorber as shown below.



POINTS

(1) Ground the surge absorber (E1) and the PC (E2) separately from each other.

(2) Select a surge absorber making allowances for power voltage rises.

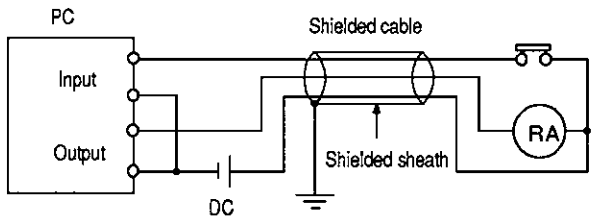
(2) Wiring of I/O equipment

(a) Applicable size of wire to the terminal block connector is 0.75(18) to 1.5 mm^2 (14 AWG). However, it is recommended to use wires of 0.75 mm^2 (18 AWG) for convenience.

(b) Separate the input and output lines.

(c) I/O signal wires must be at least 100 mm (3.94 in.) away from high-voltage and large-current main circuit wires.

(d) When the I/O signal wires cannot be separated from the main circuit wires and power wires, ground on the PC side with batch-shielded cables. Under some conditions, it may be preferable to ground on the other side.



(e) If wiring has been done with a piping, ground the piping.

(f) Separate the 24 VDC I/O cables from the 100 VAC and 200 VAC cables.

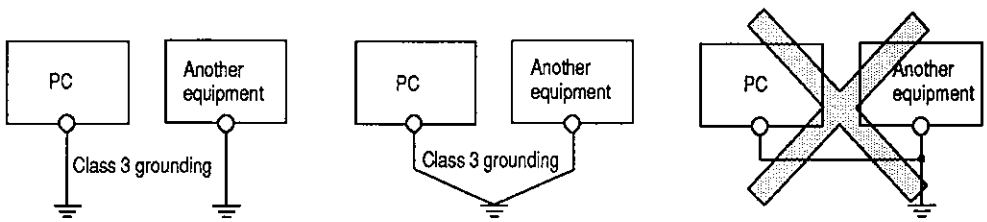
(g) If wiring over 200 m (0.12 miles) or longer distance, problems can be caused by leakage currents due to line capacity. Take corrective action as described in Section 11.4.

(3) Grounding

Grounding must be done conforming to (a) to (d) given below

(a) Ground the PC as independently as possible. Class 3 grounding should be used (grounding resistance 100 Ω or less).

(b) When independent grounding is impossible, use the joint grounding method as shown in the figure below (2).



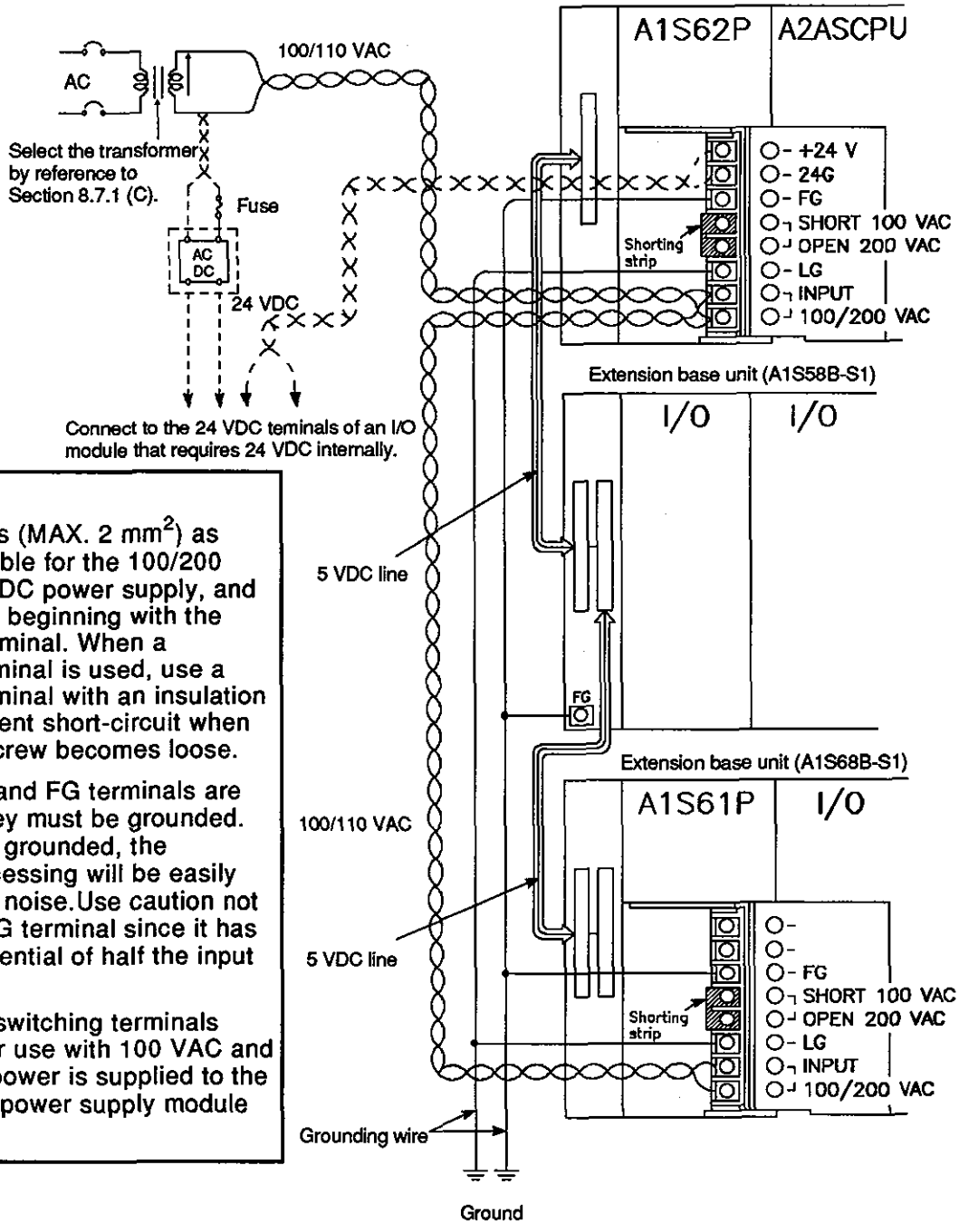
(1) Independent grounding...Best (2) Joint grounding.....Good (3) Joint grounding.....Not allowed

(c) Should incorrect operation occur due to grounding, disconnect one or both of the LG and FG terminals of base units from the grounding.

(4) The following is an example of wiring of the power supply and grounding wires to the main base unit and extension base unit.

(a) When the power supply voltage for the power supply module (A1S61P, A1S62P) is set at 100 V, put a shorting strip on the voltage switching terminals of the power supply module.
Since the voltage switching terminals are factory-set for the open state, it is not necessary to put the shorting strip when the power supply voltage 200 VAC is used.
The A2ASCPU can operate with the 85 to 264 VAC power supply voltage range without switching the voltage setting.

(b) Wiring example



POINTS

(1) Use thick wires (MAX. 2 mm^2) as much as possible for the 100/200 VAC and 24 VDC power supply, and twist the wires beginning with the connecting terminal. When a solderless terminal is used, use a solderless terminal with an insulation sleeve to prevent short-circuit when the terminal screw becomes loose.

(2) When the LG and FG terminals are connected, they must be grounded. If they are not grounded, the operation processing will be easily influenced by noise. Use caution not to touch the LG terminal since it has an electric potential of half the input voltage.

(3) If the voltage switching terminals are shorted for use with 100 VAC and if a 200 VAC power is supplied to the terminals, the power supply module will break.

9. MAINTENANCE AND INSPECTION

This chapter describes items for daily and periodic maintenance and inspection in order to maintain the programmable controller in the normal and best conditions.

9.1 Daily Inspection

Table 9.1 shows the inspection and items which are to be checked daily.

Table 9.1 Daily Inspection

No.	Check Item		Check Point	Judgment	Corrective Action
1	Base unit mounting conditions		Check for loose mounting screws and cover.	The base unit should be securely mounted.	Retighten screws.
2	Mounting conditions of I/O module, etc.		Check if the module is disengaged or the hook is securely engaged.	The hook should be securely engaged and the module should be positively mounted.	Securely engage the hook.
3	Connecting conditions		Check for loose terminal screws.	Screws should not be loose.	Retighten terminal screws.
			Check distance between solderless terminals.	Proper clearance should be provided between solderless terminals.	Correct.
			Check connectors of extension cable.	Connections should not be loose.	Retighten connector mounting screws.
4	CPU module indicator lamps	"POWER " LED	Check that the LED is ON.	ON (OFF indicates an error.)	See Section 10.4.1.
		"RUN" LED	Check that the LED is ON during RUN.	ON (OFF or flash indicates an error.)	See Sections 10.4.2 and 10.4.3.
		"ERROR" LED	Check that the LED is ON when an error occurred.	OFF (ON when an error occurred.)	See Sections 10.4.4 and 10.4.5.
		Input LED	Check that the LED turns ON and OFF.	ON when input is ON. OFF when input is OFF. (Display, which is not as mentioned above, indicates an error.)	See Section 10.4.6.
		Output LED	Check that the LED turns ON and OFF.	ON when output is ON. OFF when output is OFF. (Display, which is not as mentioned above, indicates an error.)	See Section 10.4.6.

9.2 Periodic Inspection

This section explains the inspection items which are to be checked every six months to one year. If the equipment have been moved or modified or wiring has been changed, also make the inspection.

Table 9.2 Periodic Inspection

No.	Check Item		Checking Method	Judgment	Corrective Action
1	Ambient environment	Ambient temperature	Measure with thermometer and hygrometer. Measure corrosive gas.	0 to 55°C	When PC is used inside a panel, the temperature in the panel is ambient temperature.
		Ambient humidity		10 to 90 %RH	
		Ambience		There should be no corrosive gases.	
2	Line voltage check.		Measure voltage across 100/200 VAC terminal.	85 to 132 VAC	Change supply power. Change transformer tap.
				170 to 264 VAC	
3	Mounting conditions	Looseness, play	Move the unit.	The module should be mounted securely and positively.	Retighten screws.
		Ingress of dust or foreign material	Visual check.	There should be no dust or foreign material, in the vicinity of the PC.	Remove and clean.
4	Connecting conditions	Loose terminal screws	Retighten.	Connectors should not be loose.	Retighten.
		distances between solderless terminals.	Visual check.	Proper clearance should be provided between solderless terminals.	Correct.
		Loose connector	Visual check.	Connectors should not be loose.	Retighten connector mounting screws.
5	Battery		Check battery status by mounting special auxiliary relays M9006 and M9007. Retighten battery if necessary.	Preventive maintenance	If battery capacity reduction is not indicated, change the battery when specified service life is exceeded.

9.3 Replacement of Battery

M9006 or M9007 turns ON when the voltage of battery for program backup and power failure compensation reduces.

Even if this special rely turns ON, the contents of the program and power failure compensation are not lost immediately.

However, if the ON state is overlooked, the PC contents may be lost.

Special auxiliary relays M9006 and M9007 are switched ON to indicate that the battery life has reduced to the time (minimum) indicated in Table 9.3 and it must be replaced if continued power failure RAM and /or data backup is required.

The following sections give the battery service life and the battery changing procedure.

9.3.1 Service life of battery

Table 9.3 shows the service life of battery.

Table 9.3 Battery Life

Battery Life (Total Power Failure Time) [Hr]		
Guaranteed value (MIN)	Actually applied value (TYP)	After M9006 or M9007 is turned ON
3600	9000	168

- The actually applied value indicates a typical value and the guaranteed value indicates the minimum value.

Preventive maintenance is as described below.

(1) Even if the total power failure time is less than the guaranteed value in the above table, change the battery after four to five years.

(2) When the total power failure time has exceeded the guaranteed value in the above table and M9006 has turned ON, change the battery.

9.3.2 Battery replacement procedure

When the service life of the battery has expired, replace the battery using the following procedure:

Even if the battery is removed, the memory is backed by a capacitor for some time.

However, if the replacement time exceeds the guaranteed value shown in the following table, the contents of the memory may be lost. Therefore, replace the battery as fast as possible.

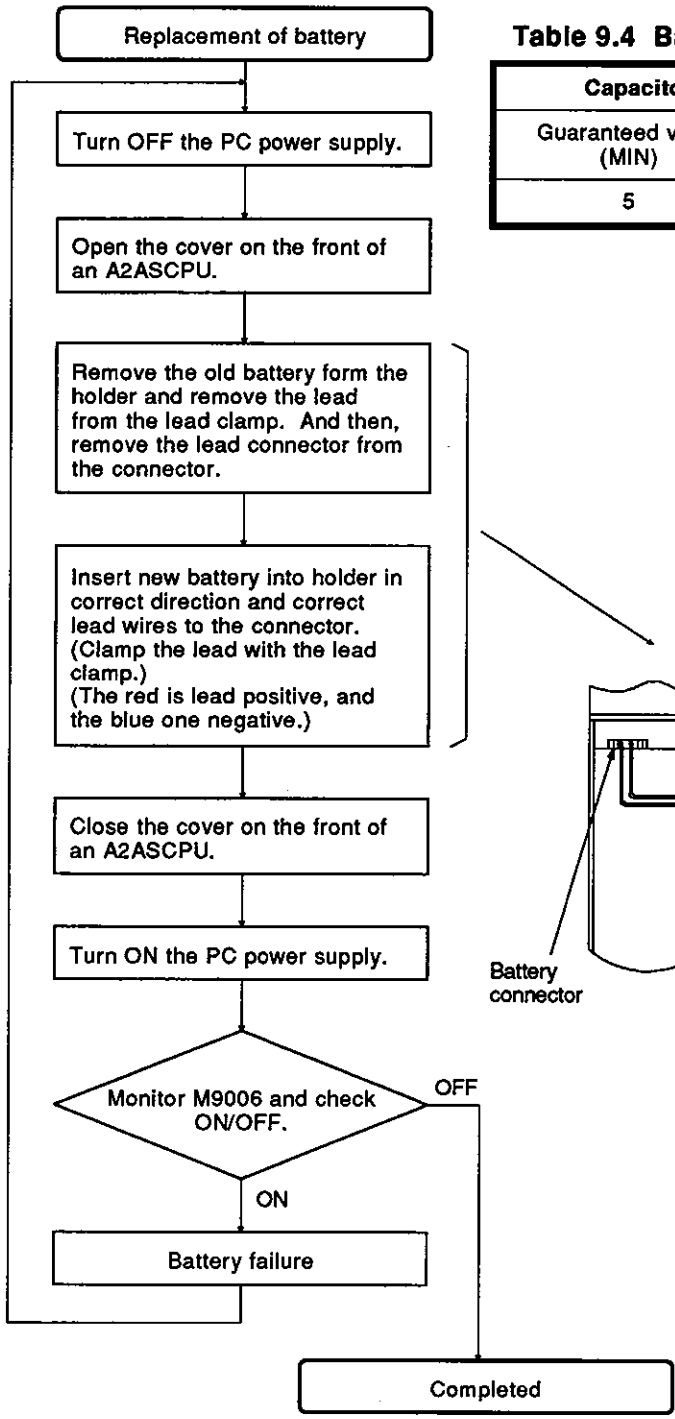
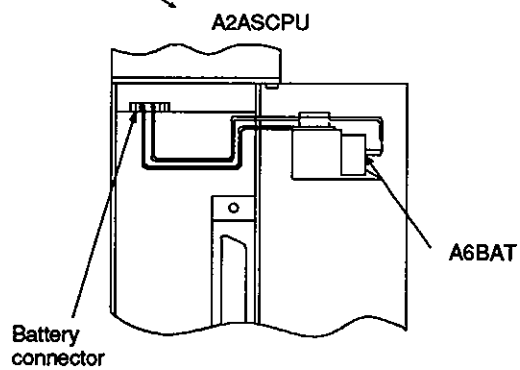


Table 9.4 Backup Time by Capacitor

Capacitor Backup Time (Minute)	
Guaranteed value (MIN)	Actually applied value (TYP)
5	15



10. TROUBLESHOOTING

This section describes various procedures for troubleshooting, as well as corrective actions.

10.1 Basic Troubleshooting

System reliability not only depends on reliable equipment but also on short down-times in the event of faults.

The three basic points to be kept in mind in troubleshooting are:

(1) Visual checks

Check the following points

(a) Machine motion (in stop and operating states)

(b) Power ON or OFF

(c) Status of I/O equipment

(d) Condition of wiring (I/O wires, cables)

(e) Display states of various indicators (such as POWER LED, RUN LED, ERROR LED, and I/O LED)

(f) States of various setting switches (such as extension base and power failure compensation)

After checking (a) to (f), connect the peripheral equipment and check the running status of the PC CPU and the program contents.

(2) Trouble check

Observe any changes in the error condition during the following:

(a) Set the RUN/STOP keyswitch to the STOP position.

(b) Reset using the RUN/STOP keyswitch.

(c) Turn the power ON and OFF.

(3) Narrow down the possible causes of the trouble

Deduce where the fault lies, i.e:

(a) Inside or outside the PC CPU.

(b) I/O module or another module.

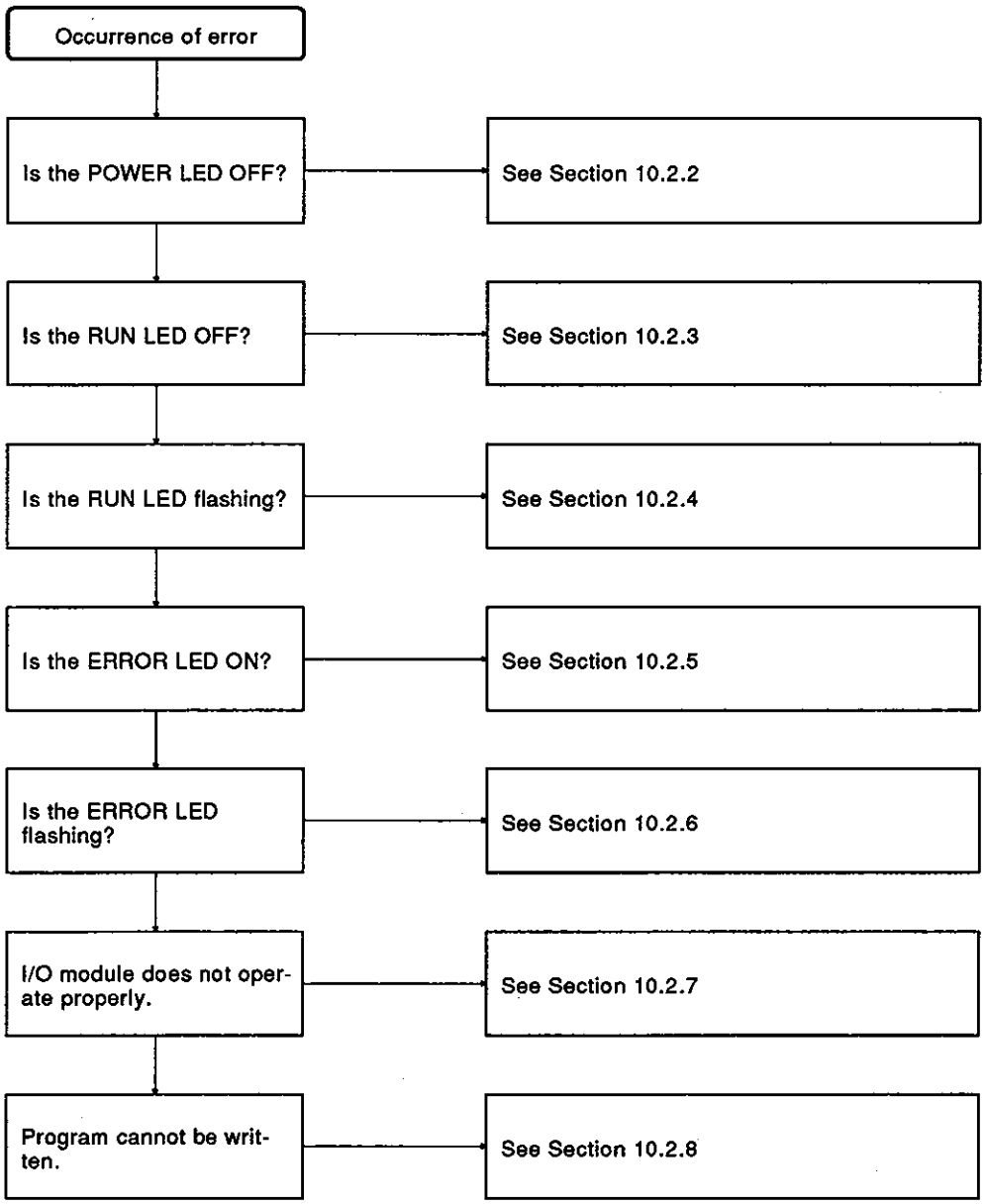
(c) Sequence program.

10.2 Troubleshooting

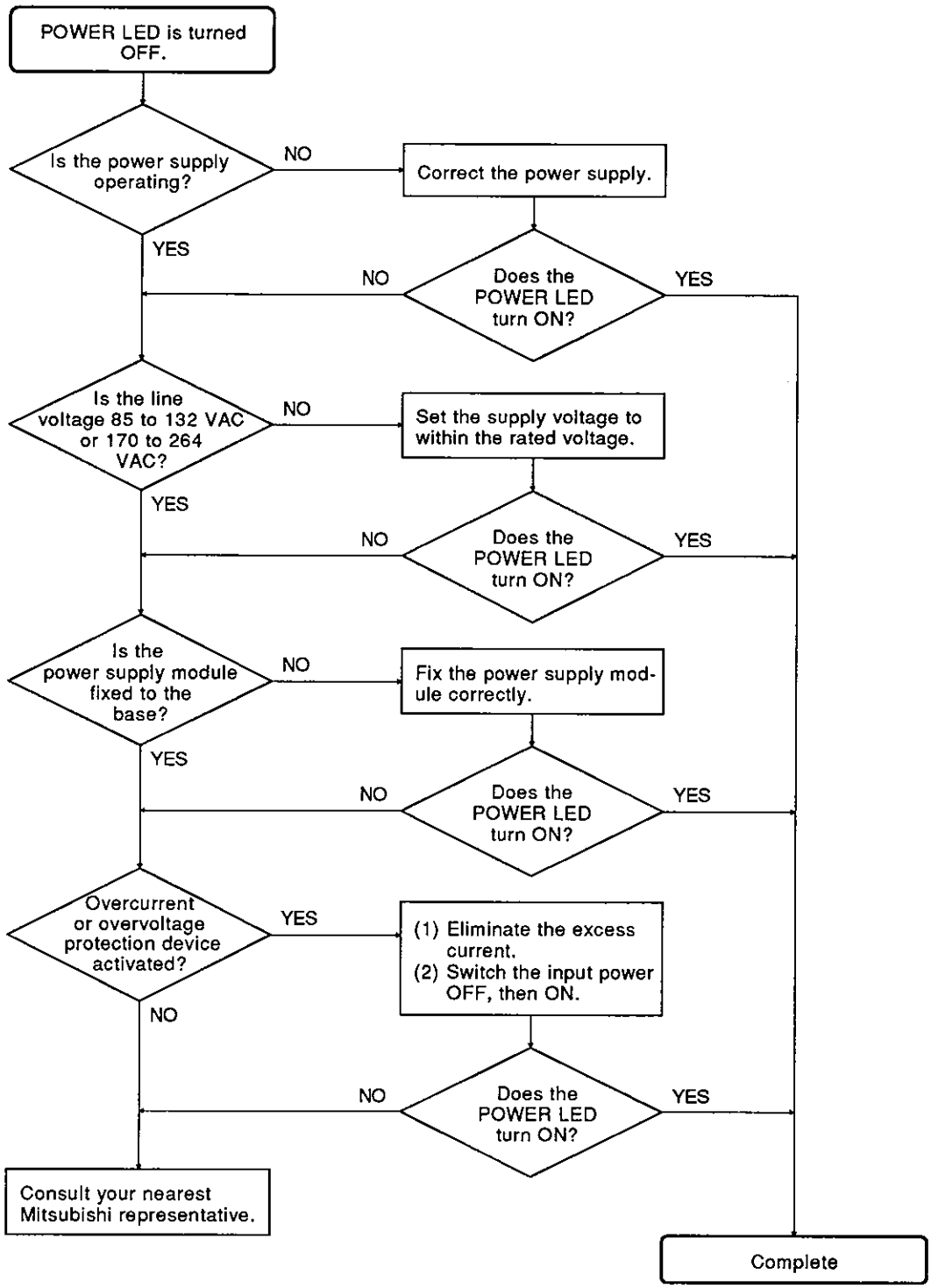
This section explains the procedure for determining the cause of problems as well as the errors and corrective actions for error codes.

10.2.1 Troubleshooting flowcharts

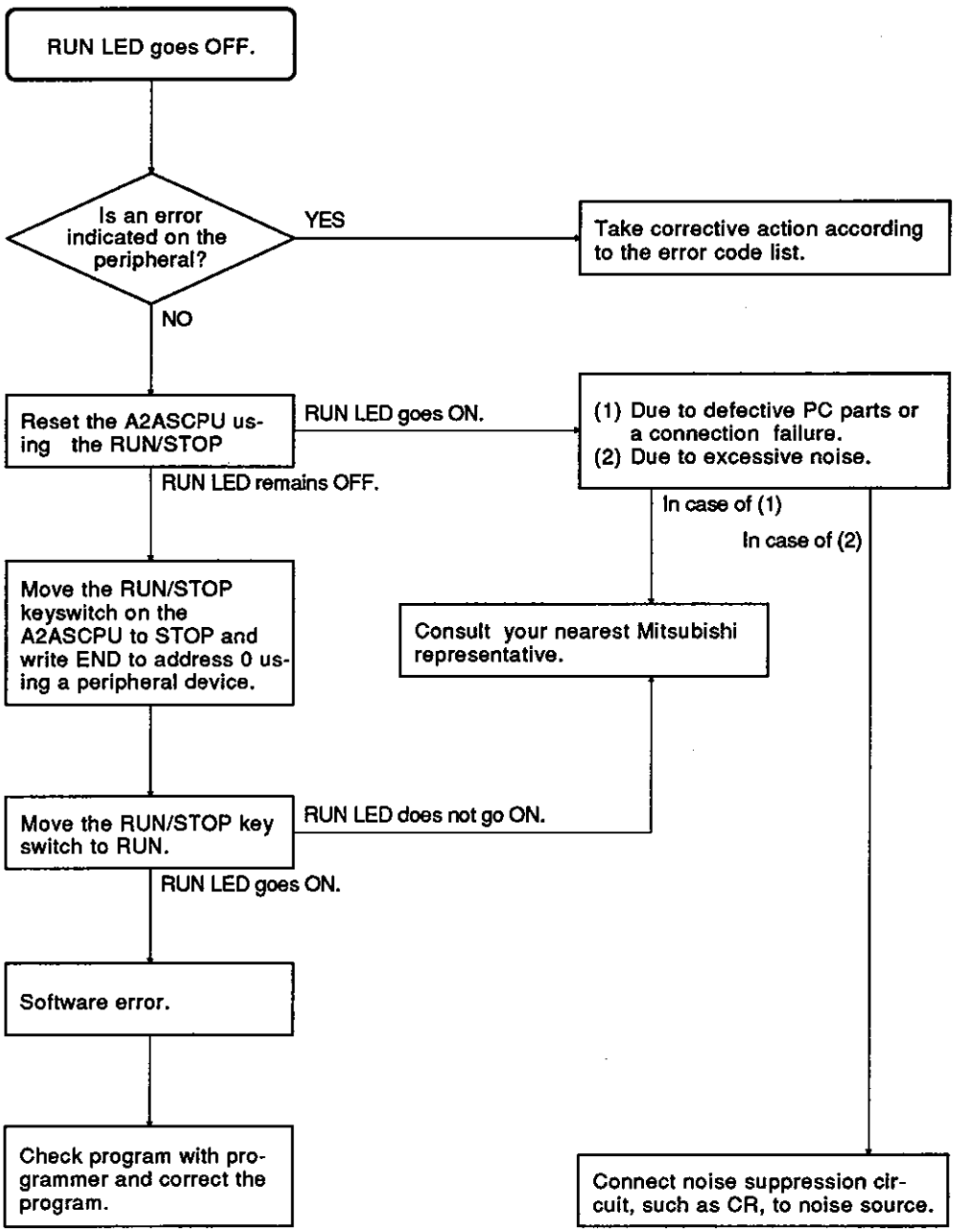
The procedures for troubleshooting are given in the following flowcharts:



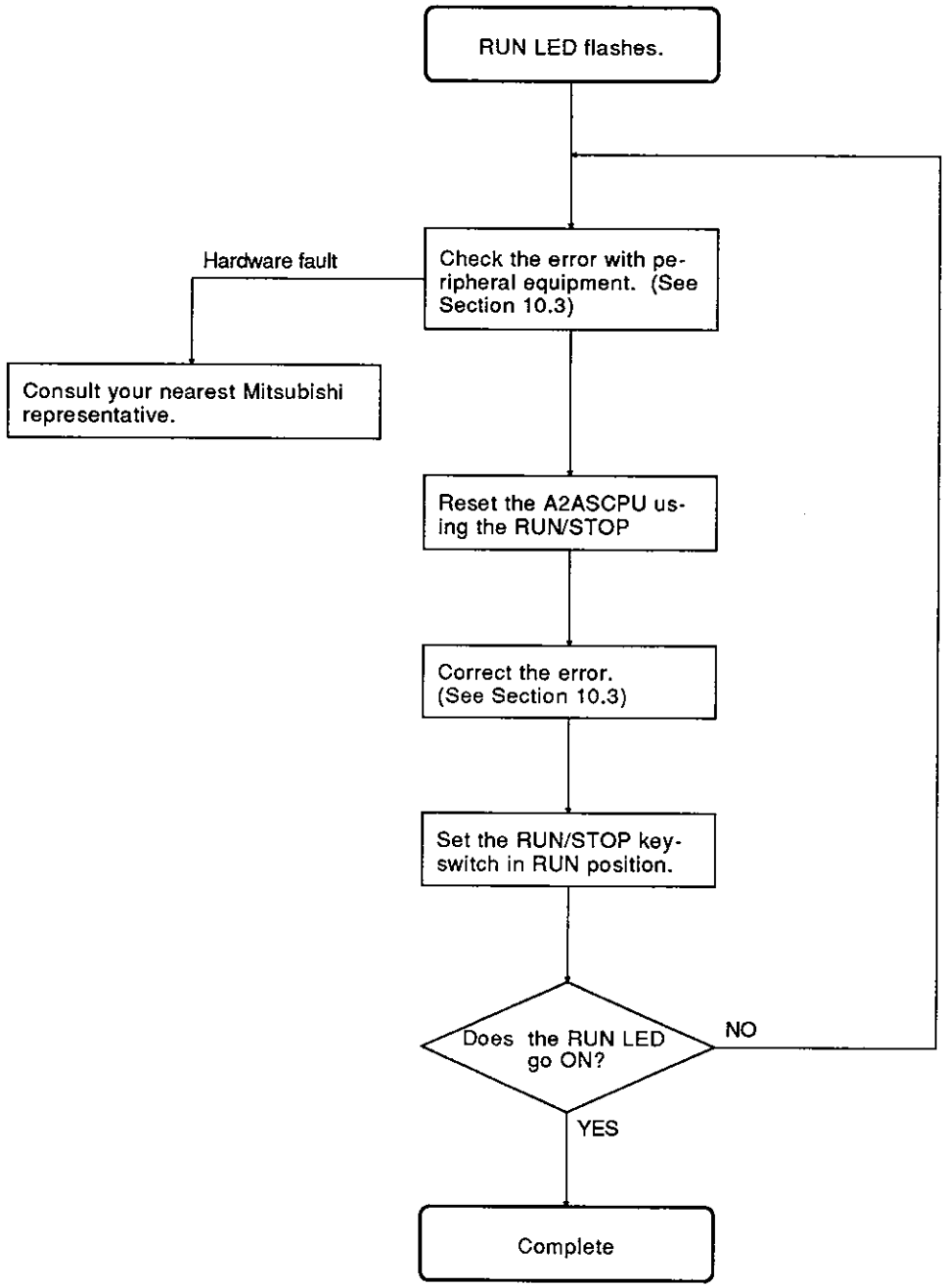
10.2.2 Flowchart used when the POWER LED goes OFF



10.2.3 Flowchart used when the RUN LED goes OFF

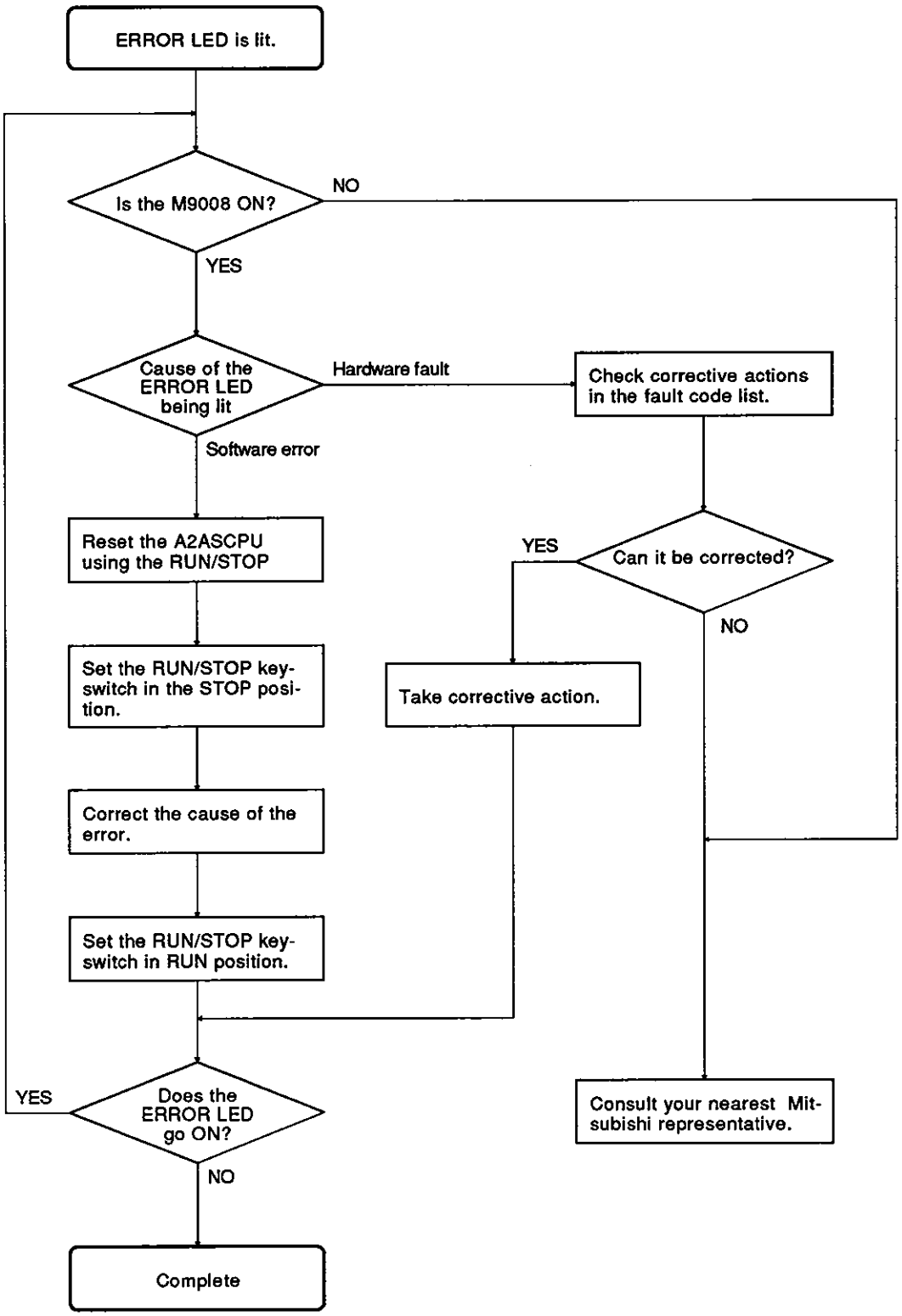


10.2.4 Flowchart used when the RUN LED flashes



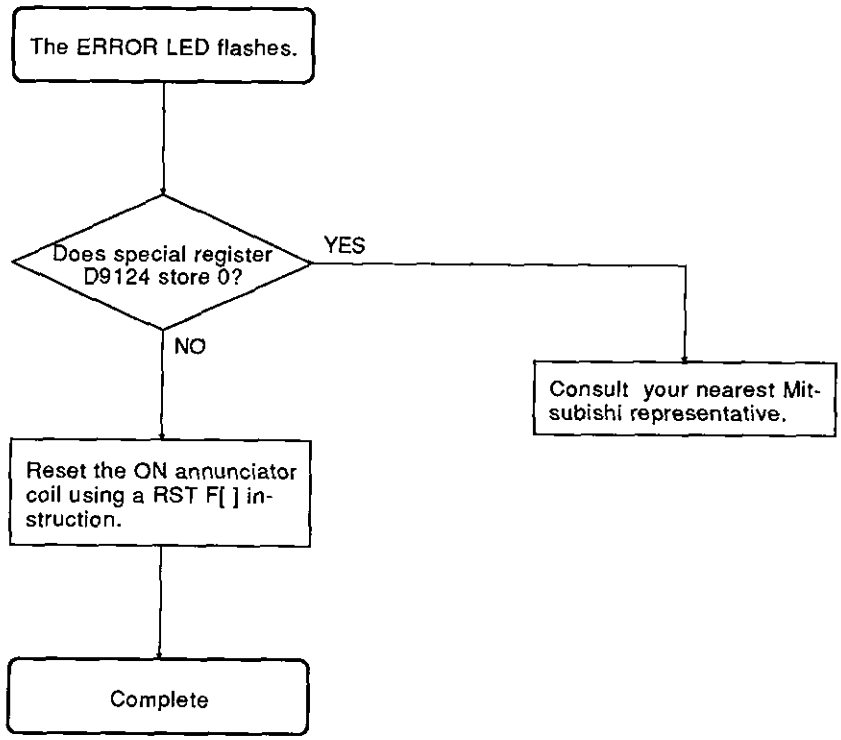
10.2.5 Flowchart used when the ERROR LED is lit

The following shows the corrective measures when the ERROR LED is lit at RUN.

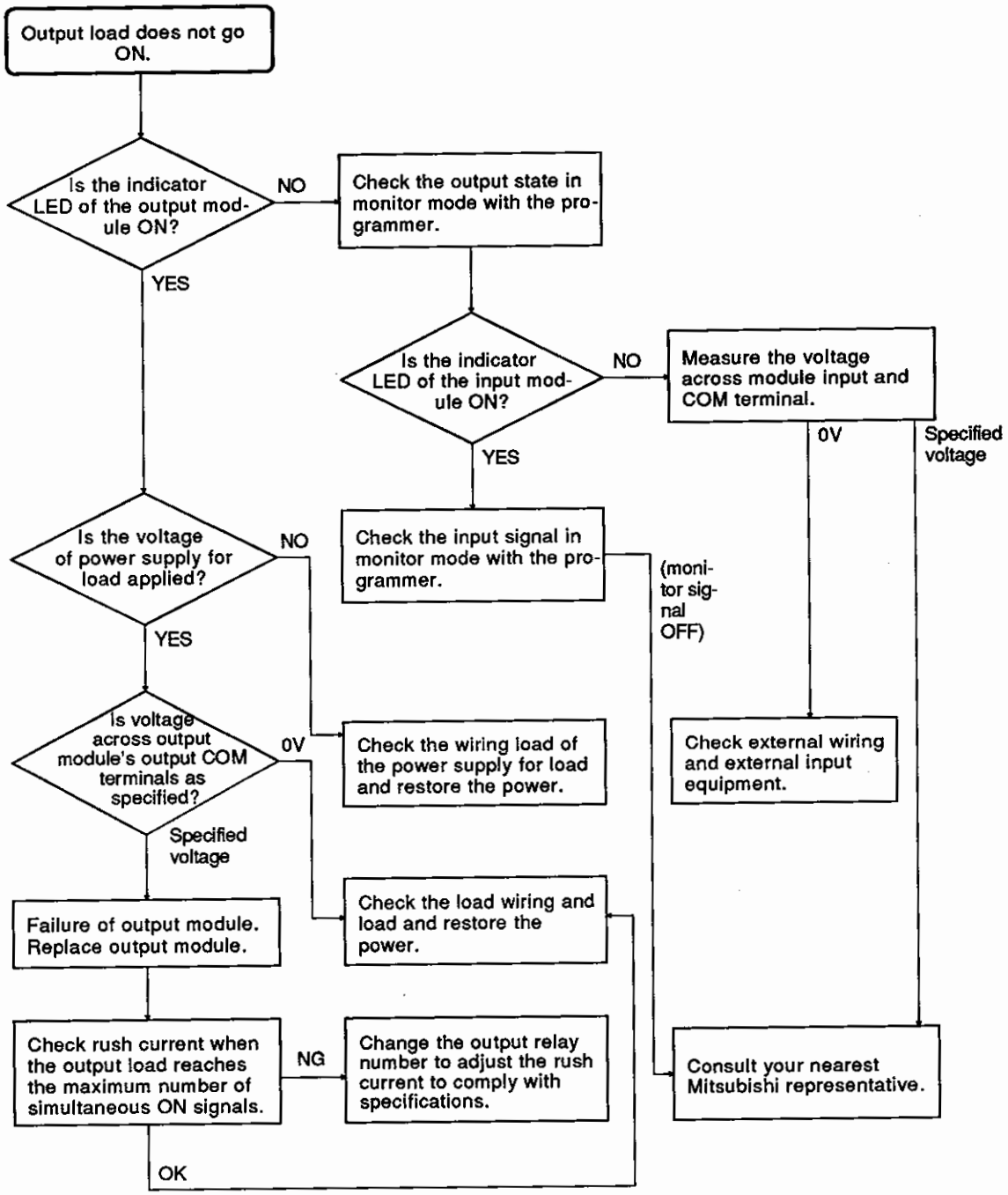


10.2.6 Flowchart used when the ERROR LED flashes

The following shows the corrective measures when the ERROR LED flashes.



10.2.7 Flowchart used when the output load of the output module does not go ON

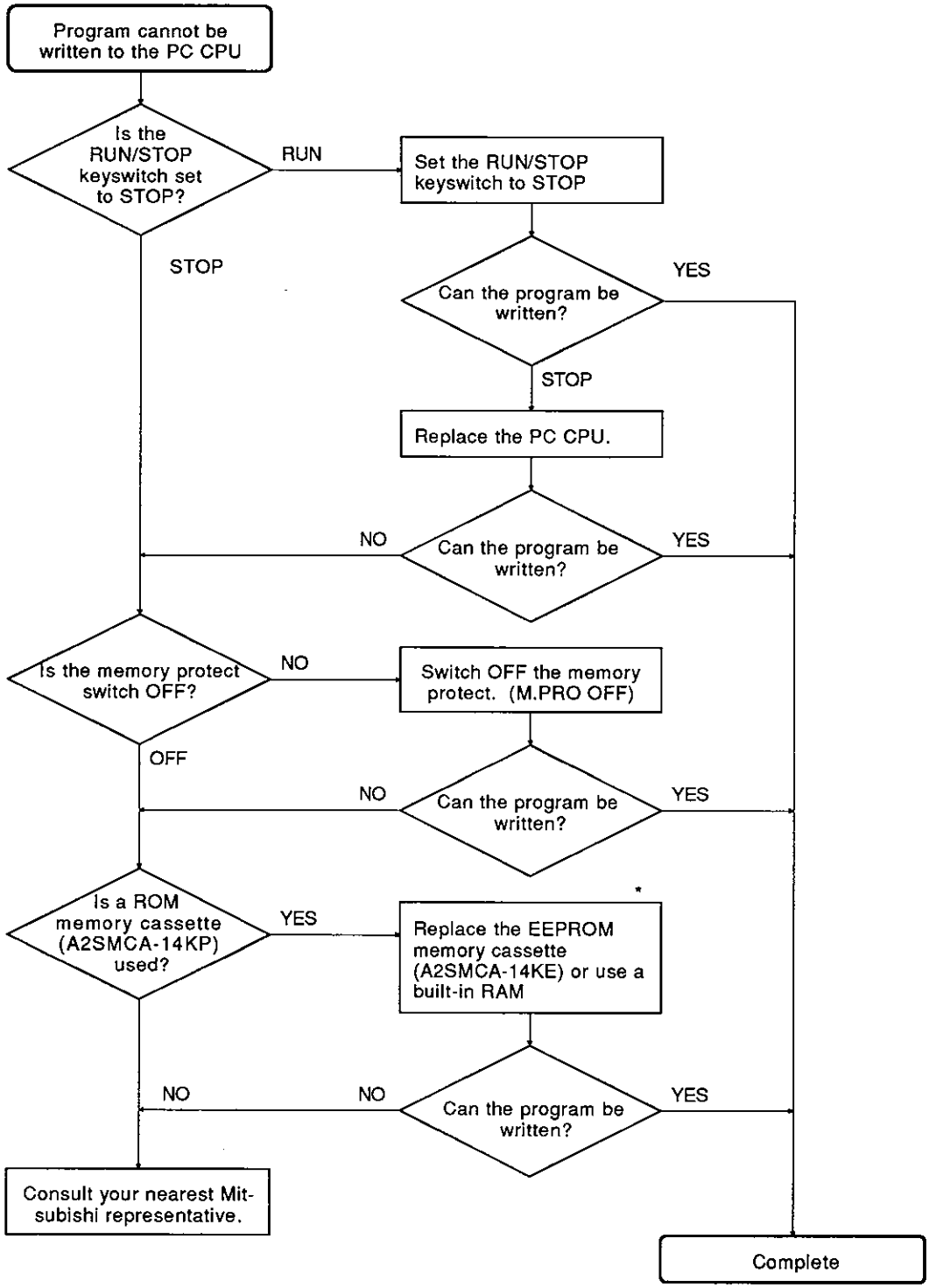


POINT

If the input or load signals are not switched OFF, see Section 10.4 and take corrective measures.

10.2.8 Flowchart used when a program cannot be written to the PC CPU

The following shows the corrective measures when a program cannot be written to the PC CPU.



* When the EEPROM memory cassette is used, make sure that the memory protect setting pins of the A2SMCA-14KE are set to OFF.

10.3 Error Code List

When an error occurs at PC RUN or during Run, the error is displayed or error code is stored in special register D9008, the detailed error code is stored in special register D9091, and the error step is stored in special register D9010 by the self-diagnostic function. The error content and corrective action are shown in Table 9.2.

10.3.1 Reading of error codes

When an error occurs, the error code can be read by peripheral device. Refer to the Peripheral Device Operating Manual for the operation method.

10.3.2 Error code list

Error codes are generated as follows:

Table 10.1 Error Code List

Error Message	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"INSTRCT CODE ERR."	10	101	An unrecognized instruction code is being used.	(1) Read the error step by peripheral device and correct the program of that step. (2) Check to see if ROM has an undecodable instruction code and replace with ROM which has the correct content.
		102	Index is qualifying for a 32-bit constant.	Read the error step by peripheral device and correct the program of that step.
		103	The device specified by extention application instruction is incorrect.	
		104	The program structure of the extension application instruction is incorrect.	
		105	The command name of the extention application instruction is incorrect.	
		106	There is a place where index qualifying with Z or V is made in the program in [LEDA/B|IX] to [LEDA/B|IXEND].	
		107	(1) The device number and set value in the OUT instruction ot the timer and counter are qualified by an index. (2) The label number of pointer (P) assigned to a destination head of [CJ], [SCJ], [CALL], [CALLP], [JMP], [LEDA/B|FCALL], [LADA/B|BREAK] instructions or the label number of interrupt pointer (I) assigned to an interrupt program head it is qualified by an index.	
(Checked at STOP → RUN or during instruction execution)		108	Error other than 101 to 107 above	

Table 10.1 Error Code List (Continued)

Error Message	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"PARAMETER ERROR" (Checked at power-on, STOP → RUN, and PAUSE → RUN)	11	111	The capacity settings of the main program, microcomputer programs, file register comments, status latch, sampling trace or extension file registers are not within the usable CPU range.	Read the parameters in the CPU memory and rewrite to the memory after checking and correcting the content.
		112	The total of the set capacities of the main program, file register comments, status latch, sampling trace and extension file registers exceed the memory cassette capacity.	
		113	The latch range in parameters or the M, L, S setting is incorrect.	
		114	Sum check error	
		115	Parameter remote RUN/PAUSE contacts, the run mode at error occurrence, the annunciator display mode or the STOP → RUN display mode setting are incorrect.	
		116	Parameter MNET-MINI automatic refresh setting is incorrect.	
		117	Parameter timer settings are incorrect.	
		118	Parameter counter settings are incorrect.	
"MISSING END INS." (Checked at STOP → RUN)	12	121	There is no END (FEND) instruction in the main program.	Write END in main program.
"CAN'T EXECUTE (P)" (Checked at the execution of instruction)	13	131	The device number of pointer (P) or interrupt pointer (I) used as the label added to the destination head is duplicating.	Remove the duplicated number of pointer (P) with the destination head and correct so that the number is not duplicated.
		132	The label of pointer (P) specified by [CJ], [SCJ], [CALL], [CALLP], [JMP], [LEDA/B|FCALL], [LEDA/B|BREAK] instructions is not specified prior to the END instruction.	Read the error step by peripheral device, check the content, and insert destination pointer (P).

Table 10.1 Error Code List (Continued)

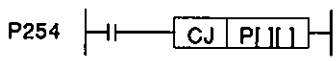
Error Message	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"CAN'T EXECUTE (P)" (Checked at the execution of instruction)	13	133	(1) Even though the [CALL] instuction is missing, the [RET] instruction has been executed since it is in the program. (2) Even though the [FOR] instruction is missing, the [NEXT] and [LEDA/B|BREAK] instructions have been executed since they are in the program. (3) Since the nesting level for the [CALL], [CALLP], or [FOR] instruction is 6 or deeper, the 6th level nest has been executed. (4) The [RET] or [NEXT] instruction is missing at execution of the [CALL] or [FOR] instruction.	(1) Read the error step by peripheral device, check the content,and correct the program at that step. (2) Nesting level fot the [CALL], [CALLP], and [FOR] instructions must be 5 or less.
		135	(1) [LEDA/B|IX] to [LEDA|IXEND] instructions are not written as a set. (2) There are more than 32 sets of [LEDA/B|IX] to [LEDA|IXEND] instructions.	(1) Read the error step by peripheral device, check the content, and correct the program at that step.' (2) [LEDA/B|IX] to [LEDA|IXEND] instructions must be less than 33 sets.
"CHK FORMAT ERR." (Checked at STOP/PAUSE → RUN)	14	141	Instructions other than LDX, LDIX, ANDX and ANIX (including NOP) are in the circuit block If the [CHK] instruction.	Refer to the content of the detailed error code, and check and correct programs related to the [CHK] instruction.
		142	There is more than 1 [CHK] instruction.	
		143	The number of contact points in the circuit block of the [CHK] instruction exceeds 150.	
		144	The [LEDA|CHK] and [LEDA|CHKEND] instructions are not written as a set, or there are 2 or more sets.	
		145	The format of the block shown below preceding the circuit block If the [CHK] instruction is abnormal. 	
		146	The D1 device number of the [CHK|D1|D2] instruction does not match the contact device number preceding the [CJP] instruction.	
		147	There is a place where index qualification is made in the check pattern circuit.	

Table 10.1 Error Code List (Continued)

Error Message	Error Code (D9008)	Detailed Error Code (D9091)	Error and Cause	Corrective Action
"CHK FORMAT ERR." (Checked at STOP/PAUSE → RUN)	14	148	(1) There is more than 1 check pattern circuit of [LEDA|CHK] to [LEDA|CHKEND] instructions. (2) There are 7 or more check condition circuits in [LEDA|CHK] to [LEDA|CHKEND] instructions. (3) The check condition circuits in [LEDA|CHK] to [LEDA|CHKEND] instructions have been created by instructions other than X and Y contact instructions and comparison instructions. (4) The check pattern circuit of [LEDA|CHK] to [LEDA|CHKEND] instructions has been created by 257 or more steps.	Refer to the content of the detailed error code, and check and correct programs related to the [CHK] instruction.
"CAN'T EXECUTE (1)" (Checked at the occurrence of interruption)	15	151	The [IRET] instruction exists outside the interrupt program and has been executed.	Read the error step by peripheral device and erase the [IRET] instruction.
		152	No [IRET] instruction in the interrupt program.	Check and correct use of [IRET] instruction inside or outside interrupt program.
		153	An interrupt module is being used though there is no corresponding interrupt pointer (I). At error occurrence, pointer (I) is stored in D9011.	Monitor special register D9011 by peripheral device, check whether or not there is an interrupt program corresponding to the stored numeric values or whether or not the same number exists for the interrupt pointer (I), and correct.
"RAM ERROR" (Checked at power-on)	20	201	Error of the CPU sequence program storage RAM	Possible hardware fault, consult Mitsubishi representative.
		202	Error of the CPU work area RAM	
		203	CPU device memory error	
		204	CPU address RAM error	
"OPE CIRCUIT ERR" (Cheked at power-on)	21	211	The operation circuit executing index qualification in the CPU is not operating normally.	Possible hardware fault, consult Mitsubishi repressentative.
		212	The CPU hardware (logic) is not operating normally.	
		213	The operation circuit executing PC sequence program in the CPU is not operating normally.	
"WDT ERROR" (Checked at the execution of END instruction)	22	——	Scan time exceeds watchdog error monitor time. (1) User program scan time has increased. (2) Momentary power failure during program scan has caused apparent scan time to increase.	(1) Check PC program scan time and reduce using the [CJ] instruction. (2) Check for momentary power failures by monitoring special register D9005.

Table 10.1 Error Code List (Continued)

Error Message	Error Code (D9008)	Detailed Error Code (d9091)	Error and Cause	Corrective Action
"END NOT EXECUTE" (Checked at end of program)	24	241	The entire stored program has been executed without executing the END instruction. (1) The END instruction has been missed (e.g. memory cassette removed during program execution). (2) The END instruction has been corrupted.	(1) Reset CPU If error persists, possible hardware fault, consult Mitsubishi representative.
"MAIN CPU DOWN"	26	———	The main CPU is malfunctioning or broken.	Possible hardware fault, consult Mitsubishi representative.
"UNIT VERIFY ERR." (Checked continuously)	31	———	Verified data is different from the I/O data at power on. (1) An I/O module (including special function module) has been removed or the base unit while the PC power is switched ON, or wrong module is loaded.	Read the detailed error code by peripheral device, check and replace the module corresponding to that numeric value (I/O head number) or monitor special registers D9116 to D9123 by peripheral device, check and replace the module where that data bit is "1".
"FUSE BREAK OFF" (Checked continuously)	32	———	Output unit fuse blown.	(1) Check the fuse blown LED indicator of the output module and replace the fuse of the lit module. (2) Read the detailed error code by peripheral device and replace the fuse of the output module corresponding to that numeric value (I/O head number), or monitor special registers D9100 to D9107 by peripheral device and replace the fuse of the output module where that data bit is "1".
"CONTROL-BUS ERR."	40	401	Incorrect FROM/TO instruction execution.	Hardware fault (CPU, special function unit and/or base unit). Consult Mitsubishi representative.
		402	Parameter I/O assignment, special function modules cannot be accessed at initial communication. At error occurrence, the head I/O number (the upper 2 digits of a 3 digit expression) of the special function module causing the error is stored in D9011.	
"SP. UNIT DOWN"	41	411	No response from special function unit after execution of FROM/TO instruction.	Hardware error of the accessed special function module. Consult Mitsubishi representative.
		412	During parameter I/O assignment, at initial communication, responses from special function modules have not been returned. At error occurrence, the head I/O number (the upper 2 digits of a 3-digit expression) of the special function module causing the error is stored in D9011.	
"LINK UNIT ERROR"	42	———	Two A1SJ71AP21/R21, A1SJ71AT21B, AJ71AP21/R21, or AJ71AT21Bs are set as master stations.	Set one as a master station and one as a local station.

Table 10.1 Error Code List (Continued)

Error Message	Error Code (D9008)	Detailed Error Code (d9091)	Error and Cause	Corrective Action
"I/O INT. ERROR"	43	———	Interrupt signal received with no interrupt module present.	Since a hardware error has occurred in one of the modules, replace the modules one by one to find the faulty module. Consult Mitsubishi representative.
"SP. UNIT LAY. ERR."	44	441	I/O modules allocated in parameter settings by peripheral device have been allocated by special function modules. Or, the opposite settings have been executed.	Reset I/O assignments in parameters by peripheral device according to the loading status of the special function modules.
		442	More than 8 special function modules [except for the AI61 (S1)/A1SI61] which can start interrupts to the CPU have been loaded.	Load less than 9 special function modules [except for the AI61 (S1)/A1SI61] which can start interrupts to the CPU.
		443	More than 1 AJ71AP21/R21s has been loaded.	Load less than 2 AJ71AP21/R21s.
		444	More than 6 computer link modules, etc., have been loaded to 1 CPU module.	Load less than 7 computer link modules.
		445	More than 1 AI61 (S1)/A1SI61 has been loaded.	Load only 1 AI61/A1SI61.
		446	The modules MNET/MINI automatic refresh allocated in parameter settings by peripheral device and the names of the modules of actually linked station numbers are incorrect.	Reset the module assignments of the MNET/MINI automatic refresh in parameter settings by peripheral device according to the modules of station numbers actually linked.
		447	The number special function modules which can use dedicated instructions, registered by I/O assignment per one CPU module (number of modules to be loaded) is larger than the specified limit. (The total of computers shown below is 1344 or more.) (Number of loaded AD59 x 5) (Number of loaded AD57(S1)/AD58 x 8) (Number of loaded AJ71C24(S3/S6/S8) x 10) (Number of loaded AJ71UC24 x 10) (Number of loaded AJ71C21(S1) x 29) + (Number of loaded AJ71PT32(S3) x 125) Total > 1344	Decrease the number of loaded special function modules.

Table 10.1 Error Code List (Continued)

Error Massage	Error Code (D9008)	Detailed Error Code (d9091)	Error and Cause	Corrective Action
"SP. UNIT ERROR" (Checked when FROM/TO instruction, or special function module dedicated instruction is specified.)	46	461	There is no special function module in the area specified by the FROM/TO instruction.	Read the error step by peripheral device, check and correct the content of the FROM/TO instruction of that step.
		462	There is no special function module in the area specified by the FROM/TO instruction or there is no corresponding special function module.	Read the error step by peripheral device, check and correct the content of the special function module dedicated instruction of that step.
"LINK PARA. ERROR"	47	———	(1) The link range is set in parameter settings by peripheral device, and for some reason, the content written to the link parameter area differs from the link parameter content read by the CPU or link parameter is not written. (2) 0 slave stations set.	(1) Re-write link parameters from peripheral programming unit to PC. (2) Check station number setting. (3) Persistent error occurrence may be an indication of hardware fault. Consult Mitsubishi representative.
"OPERATION ERROR" (Checked during execution of instruction)	50	501	(1) When using file register (R), operations have been executed exceeding the specified range for the device number and block number of file register (R). (2) The file register is used in the program without executing file register capacity settings.	Read the error step by peripheral device, check and correct the program of that step.
		502	The combination of devices specified by instruction is incorrect.	
		503	The storage data of specified devices or the constants are not within the usable range.	
		504	The quality of settings used for handled data has exceeded the usable range.	
		505	(1) The station number specified by instruction [LEDA/B|LRDP], [LEDA/B|LWTP], [LRDP] or [LWTP] is not a local station. (2) The head I/O number specified by instruction [LEDA/B|RFRP], [LEDA/B|RTOP], [RFRP] or [RTOP] is not a remote station.	
		506	The head I/O number specified by instruction [LEDA/B|RFRP], [LEDA/B|RTOP], [RFRP] or [RTOP] is not a special function module.	

Table 10.1 Error Code List (Continued)

Error Message	Error Code (D9008)	Detailed Error Code (d9091)	Error and Cause	Corrective Action
"OPERATION ERROR" (Checked during execution of instruction)	50	507	(1) While the AD57 (S1) or the AD58 is executing instructions by partial processing, other instruction have been output to the same module. (2) While the AD57 (S1) or the AD58 is executing instructions by partial processing, instructions have been output to other AD57 (S1) or AD58 by partial processing.	Read the error step by peripheral device and provide interlock by special relay M9066 or change the program structure and correct. This prevents the execution of other instructions to the same module while executing instructions to the AD57 (S1) or AD58 by partial processing and prevents the execution of instructions to other AD57(S1) or AD58 by partial processing.
		509	(1) An instruction which cannot be executed by remote terminal module connected to the MNET/MINI-S3 was executed to the modules. (2) When the [PRC] instruction was executed to a remote terminal, the communication request registration areas overflowed. (3) The [PIDCONT] instruction was executed without executing the [PIDINIT] instruction. The [PID57] instruction was executed without executing the [PIDINIT] or [PIDCONT] instruction.	(1) Read the error step by peripheral device and correct the program, meeting loaded conditions of remote terminal module. (2) Provide interlock using M9081 (communication request registration areas BUSY signal) or D9081 (number of vacant areas in the communication request registration areas) when the [PRC] instruction is executed to a remote terminal. (3) Execute each instruciton, and then, execute the next in struction.
"MAIN CPU DOWN"	60	———	(1) INT instruction processed in microcomputer program area. (2) CPU malfunction due to noise. (3) Hardware fault.	(1) Remove INT. (2) Eliminate noise. (3) Hardware fault.
"BATTERY ERROR" (Checked at power-on)	70	———	(1) Battery voltage low. (2) Battery not connected.	(1) Replace the battery. (2) When using RAM memory or the power failure compensation function, load the lead connectors.

10.4 I/O Connection Troubleshooting

This section explains possible problems with I/O circuits.

10.4.1 Input circuit troubleshooting

This section describes possible problems with input circuits, as well as corrective actions.

Table 10.2 Input Circuit Problems and Corrective Actions

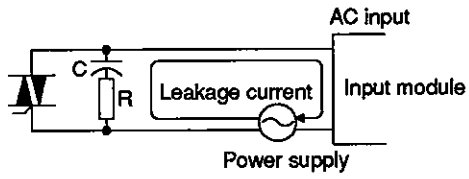
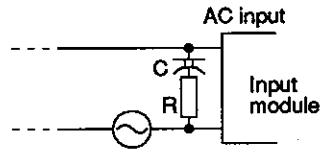
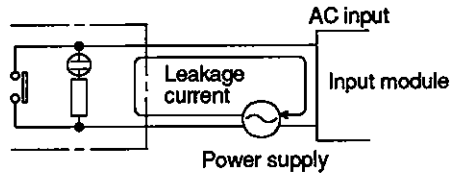
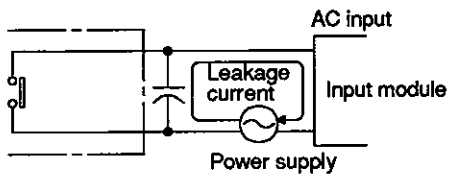
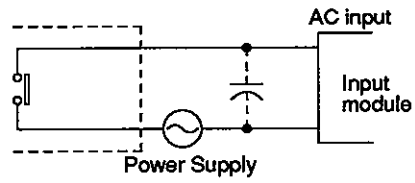
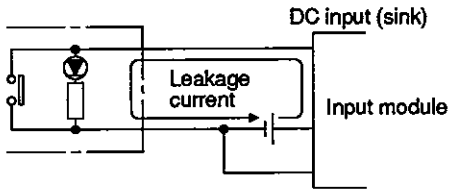
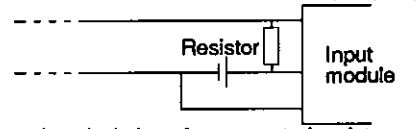
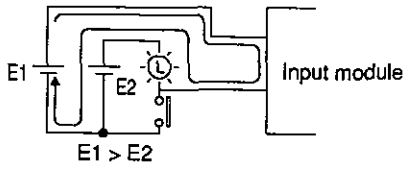
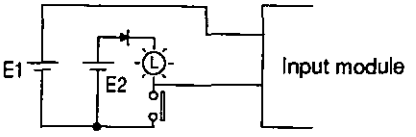
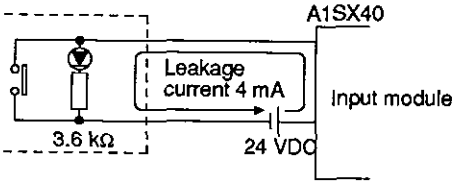
	Condition	Cause	Corrective Action
Example 1	Input signal does not turn OFF.	Leakage current of input switch (such as a drive by non-contact switch). 	• Connect an appropriate register which will make the voltage across the terminals of the input module lower than the OFF voltage value.  It is recommended to use 0.1 to 0.47 μF + 47 to 120 Ω (1/2 W) for the constant.
Example 2	Input signal does not turn OFF.	Drive by a limit switch with neon lamp. 	• Same as Example 1. • Or make up another independent display circuit.
Example 3	Input signal does not turn OFF.	Leakage current due to line capacity of wiring cable. Line capacity C of twisted pair wire is approx. 100 PF/m). 	• Same as Example 1. • However, leakage current is not generated when power supply is located on the input equipment side as shown below. 
Example 4	Input signal does not turn OFF.	Drive by switch with LED indicator. 	• Connect a register which will make the voltage across input module terminal and common higher than the OFF voltage, as shown below.  * A sample calculation of a connected resistor value is given on the following page.

Table 10.2 Input Circuit Problems and Corrective Actions (Continued)

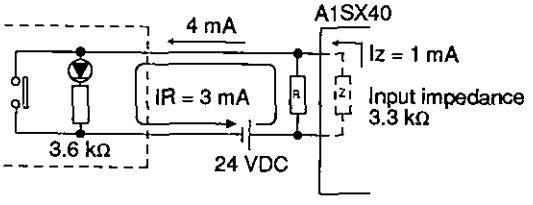
	Condition	Cause	Corrective Action
Example 5	Input signal does not turn OFF.	• Sneak path due to the use of two power supplies. 	• Use only one power supply. • Connect a sneak path prevention diode. (Figure below) 

Sample calculation for Example 4

The switch with the LED indicator is connected to A1SX40 and there is a 4 mA leakage current.



(1) Since this voltage does not satisfy the OFF voltage of 1 [mA] or lower, the input signal does not go OFF. Therefore, connect a resistor as shown below.



(2) Calculate the resistance value of R as follows:
To obtain the 1 mA OFF current for the A1SX40, a 3 mA current or larger must flow to R.

$I_R : I_Z = Z$ (input impedance) : R

$$R \leq \frac{I_Z}{I_R} \times (\text{input impedance}) = \frac{1}{3} \times 3.3 = 1.1\ [k\Omega]$$

$$R < 1.1K\Omega$$

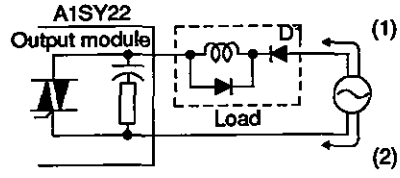
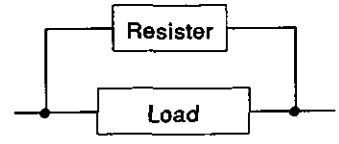
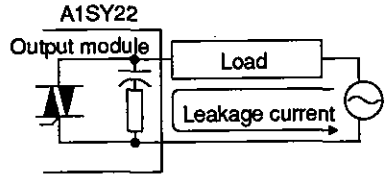
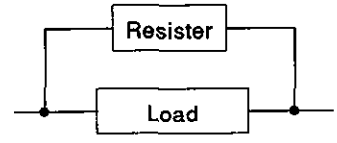
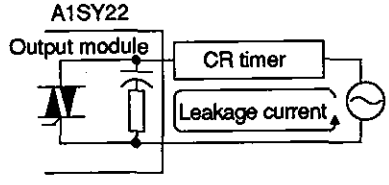
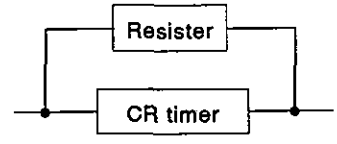
If the resistance value of R is 1 kΩ, the power capacity W of the resistor R is calculated as follows:

$$W = (\text{current value})^2 \times R = 0.003^2\ (A) \times 1000\ (\Omega) = 0.009\ (W)$$

(3) Since the power capacity of the resistor is usually selected as 3 to 5 times the actual power consumption, a 1 kΩ 0.5 W resistor must be connected to the terminals concerned.

10.4.2 Output circuit failures and corrective actions

Table 10.3 Output Circuit Failures and Corrective Actions

	Condition	Cause	Corrective Action
Example 1	When the output is OFF, excessive voltage is applied to the load.	• Load is half-wave rectified inside (in some cases, it is true of a solenoid).  • When the polarity of the power supply is as shown in [1], C is charged. When the polarity is as shown in [2], the voltage charged in C plus the line voltage are applied across D1. Max. voltage is approx. 2.2E.	• Connect a resistor of 10 to 99 kΩ. across the load. (If a resistor is used in this way, it does not pose a problem to the output element. But it may cause the diode, which is built in the load, to deteriorate, resulting in a fire, etc.) 
Example 2	The load does not turn OFF (triac output).	• Leakage current due to built-in noise suppression 	• Connect C and R across the load. (When the wiring distance from the output card to the load is long, there may be a leakage current due to the line capacity.) 
Example 3	When the load is a C-R type timer, time constant fluctuates (triac output).		• Drive the relay using a contact and drive the C-R type timer using the same contact. (Some timers have half-wave rectified internal circuits. Therefore, take the precautions indicated in the example.)  Calculate the CR constant depending on the load.

11. DEVICES AND INSTRUCTIONS

11.1 Special Relay List

Special relays are internal relays whose uses are determined inside the PC. Therefore, they cannot be turned ON/OFF as coils is a program. (Except for *1 and *2 in the table)

Table 11.1 Special Relay List

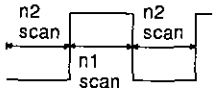
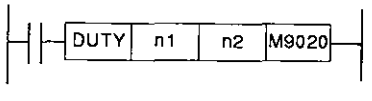
Number	Name	Description	Details
*1 M9000	Fuse blown	OFF: Normal ON: Presence of fuse blow module	• Turned ON when there is one or more output modules of which fuse has been blown. Remains ON if normal status is restored.
*1 M9002	I/O module verify error	OFF: Normal ON: Presence of error	• Turned ON if the status of I/O module is different from enterd status when power is turned on. Remains ON if normal status is restored.
*1 M9004	MINI link error	OFF: Normal ON: Error	• Turns ON when a unit detects an error in the master station of the MINI link. Remains On after the error is corrected.
*4 M9005	AC DOWN detection	OFF: AC is good ON: AC is down	• Turned ON if power failure of within 20 msec occurs. Reset when POWER switch is moved from OFF to ON position.
M9006	Battery low	OFF: Normal ON: Battery low	• Turned ON when battery voltage reduced to less than specified. Turned OFF when battery voltage becomes normal.
*1 M9007	Battery low latch	OFF: Normal ON: Battery low	• Turned ON when battery voltage reduces to less than specified. Remains ON if battery voltage becomes normal.
*1 M9008	Self-diagnosistic error	OFF: Absence of error ON: Presence of error	• Turned ON when error is found as a result of self-diagnosis.
M9009	Annunciator detection	OFF: Absence of detection ON: Presence of detection	• Turned ON when OUT F or SET F instruction is executed. Switched OFF when D9124 value is set to 0.
*1 M9011	Operation error flag	OFF: Absence of error ON: Presence of error	• Turned On when operation error occurs during execution of application instruction. Remains ON if normal status is restored.
M9012	Carry flag	OFF: Carry off ON: Carry on	• Carry flag used in application instruction
M9016	Data memory clear flag	OFF: No processing ON: Output clear	• Clears all data memory (except special relays and special registers) in remote run mode from computer, etc. when M9016 is 1.
M9017	Data memory clear flag	OFF: No processing ON: Output clear	• Clears all data memory (except special relays and special registers) in remote run mode from computer, etc. when M9017 is 1.
M9020	User timing clock No. 0		• Relay which repeats ON/OFF at intervals of predetermined scan. • When power is turned ON or reset is performed, the clock starts with OFF. • Set the intervals of ON/OFF [DUTY] instruction. 
M9021	User timing clock No. 1		
M9022	User timing clock No. 2		
M9023	User timing clock No. 3		
M9024	User timing clock No. 4		
*2 M9025	Clock data set request	OFF: No processing ON: Data set request	• Writes clock data from D9025 to D9028 to the clock devices after the END inistrucion is executed at the scan when M9025 is switched on.

Table 11.1 Special Relay List (Continued)

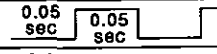
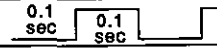
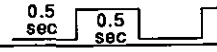
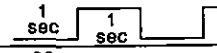
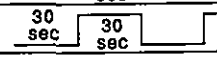
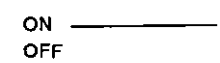
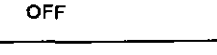
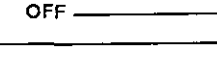
Number	Name	Description	Details
M9026	Clock data error	OFF: No error ON: Error	• Switched ON when a clock data (D9025 to D9028) error occurs.
*2 M9028	Clock data read request	OFF: No processing ON: Read request	• Reads clock data in BCD to D9025-D9028 when M9028 is switched ON.
*2 M9029	Data communication request batch processing	OFF: Batch processing is not executed. ON: Batch processing is executed.	• By turning ON M9029 by using a sequence program, all requests of data communication accepted during 1 scan are processed by END proccessing of the scan. • Data communication request batch processing ON/OFF can be switched during RUN. • Default is OFF. (Data communication requests are processed one at a time by each END processing in the order that they are accepted.
M9030	0.1 second clock		• 0.1 second, 0.2 second, 1 second, 2 second, and 1 minute clocks are generated. • Not turne ON and OFF per scan but turned ON and OFF even during scan if corresponding time has elapsed. • Starts when power is turned ON or reset is performed.
M9031	0.2 second clock		
M9032	1 second clock		
M9033	2 second clock		
M9034	1 minute clock		
M9036	Normally ON		• Used as dummy contacts of initialization an application instruction in sequence program. • M9036 and M9037 are switched ON/OFF independently of the CPU RUN/STOP switch position. M9038 and M9039 are switched ON/OFF in accordance with the RUN/STOP switch position, i.e. switched OFF when the switch is set to STOP. When the switch is set to other than STOP, M9038 is only switched ON during 1 scan and M9030 is only switched OFF during 1 scan.
M9037	Normally OFF		
M9038	ON only for 1 scan after RUN		
M9039	RUN flag (OFF only for 1 scan after RUN)		
M9040	PAUSE enable coil	OFF: PAUSE disabled ON: PAUSE enabled	• When RUN key switch is at PAUSE position or REMOTE PAUSE contact has turned ON and if M9040 is ON, PAUSE mode is set and M9041 is turned ON.
M9041	PAUSE status contact	OFF: During PAUSE ON: Not during PAUSE	
M9042	STOP status contact	OFF: During STOP ON: Not during STOP	• Switched ON when the RUN/STOP switch is set to STOP.
M9043	Sampling trace completion	OFF: During sampling trace ON: Sampling trace completion	• Turned ON upon completion of sampling trace performed the number of times set in peripheral devices aftr [STRA] instruciton is executed. Reset when [STRAR] instruciton is executed.
M9044	Sampling trace	0→1: Same as [STRA] execution 1→0: Same as [STRAR] execution	• Has the same functions as the [STRA] and [STRAR] instructions. (M9044 is forced to switch ON/OFF by the peripheral device.) When switched OFF, M9044 provides the same function as the [STRA] instruciton. When switched OFF, M9044 provides the same function as the [STRAR] instruction. At this time, the sampling trace condition is based on the value in D9044. (0 for scan, time for time (10 msec increments))
M9045	Watching timer (WDT) reset	OFF: WDT is not reset ON: WDT is reset	• When M9045 is ON, WDT is reset when a ZCOM instruction and data communication request batch processing are executed. (This is used when the scan time exceeds 200 msec.

Table 11.1 Special Relay List (Continued)

Number	Name	Description	Details
M9046	Sampling trace	OFF: Except during trace ON: During trace	• On during sampling trace
M9047	Sampling trace preparation	OFF: Sampling trace stop ON: Sampling trace start	• Sampling trace is not executed until M9047 is turned ON. By turning OFF M9047, sampling trace is stopped.
M9049	Number of characters output switching	OFF: Characters up to NUL code output ON: 16 characters output	• When M9049 is OFF, characters up to NUL (00H) code are output. • When M9049 is ON, ASCII codes for 16 characters are output.
M9051	CHG instruciton execution disable	OFF: Disable ON: Enable	• Switch ON to disable CHG instruction. • Switch ON to request program transfer. Automatically switched OFF on completion of the transfer.
*2 M9052	SEG instruction switching	OFF: 7SEG display ON: I/O partial refresh	• Serves as an I/O partial refresh instruciton when M9052 is ON. Serves as a 7SEG display instruction when M9052 is OFF.
M9054	STEP RUN flag	OFF: Not during STEP RUN ON: During STEP RUN	• Switched ON when the RUN/STOP switch is in STEP RUN.
M9055	Status latch completion flag	OFF: Uncompleted ON: Completed	• Turned ON when status latch is completed. Turned OFF by reset instruction.
M9065	Division processing execution detection	OFF: Not during divided processing ON: During divided processing	• ON while an instruction to the AD57 (S1), AD58 is executed in divided processing. Turns OFF at completion of execution (no divided processing).
*2 M9066	Divided processing request flag	OFF: Batch processing ON: Divided processing	• Since instructions with long processing times to the AD57 (S1) and AD58 greatly extend the scan time, divided processing of these instructions is executed by turning M9066 ON.
M9081	Communication request entry areas BUSY signal	OFF: Communication request entry areas available ON: Communication request entry areas no available	• 32 entry areas are provided for FROM/TO instruction waiting for execution to MNET/MINI(-S3); turns ON if there are no empty areas.
*2 M9084	Error check setting	OFF: Error checked ON: Error unchecked	• Used to set whether or not the following error checks are made at the execution of the END instruction. (To shorten the END instruction processing time) • Fuse blown, I/O unit verify error, battery error
*1 M9091	Instruction error flag	OFF: No error ON: Error	• Turns ON by instruction-related error. Remains ON after the error is corrected.

Table 11.1 Special Relay List (Continued)

Number	Name	Description	Detailes
*2*3 M9094	*I/O change flag*	OFF: Changed ON: Not changed	• I/O module may be changed in online mode by switching M9094 on after the head I/O number of the new module is set to D9094. (Only one module may be changed by one setting.) • To execute I/O change during RUN, turn it ON by using a program or test mode by peripheral device. To execute I/O change during STOP, turn it ON by using test mode by peripheral device. • RUN/STOP mode must not be changed until I/O module change is complete.
M9100	Existence of SFC program	OFF: SFC program does not exist ON: SFC program exists	• *Turns ON when an SFC program has been* registered and an SFC program work area has become available. • Turn OFF when an SFC program has not been registered or when an SFC program work area is not available.
*2 M9101	SFC program start/stop	OFF: SFC program stop ON: SFC program start	• *Turned* ON by the user when starting the SFC program. When turned OFF, the operation output for the execution step is turned OFF, and the SFC program stops.
*2 M9102	SFC program start status	OFF: Initial start ON: Continued start	• Using M9101, the starting step when the SFC program is restarted is selected. ON: All execution conditions at a stop of the SFC program are cleared, and the program is restarted with block 0. OFF: Program is restarted from the execution step in the execution block at the time of stop. • Once this is turned ON, the state is latched (at power failure) by the system.
*2 M9103	Continuous transfer *setting*	OFF: Continuous transfer not provided ON: *Continuous transfer* provided	• When continuous step transfer conditions are all established, whether or not the execution of steps in which all transfer conditions in one scan are established is performed is selected. ON: Continuously executed. (Continuous transfer provided) OFF: Executed per step per scan. (Continuous transfer not provided)
M9104	Continuous transfer prevention flag	OFF: At transfer completion ON: When transfer is not executed	• Turns ON when the continuous transfer is provided and continuous transfer has not been executed. *Turns OFF when a transfer* of one step is completed. By writing M9104 by using an AND condition as the transfer condition, continuous transfer of corresponding step can be prevented.

Table 11.1 Special Relay List (Continued)

Number	Name	Description	Detailes
*2 M9108	Step transfer monitoring timer start (corresponds to D9108)	OFF: Monitoring timer reset ON: Monitoring timer reset start	• Turns ON to start a step transfer monitoring timer. Monitoring timer is reset when this is turned OFF.
*2 M9109	Step transfer monitoring timer start (corresponds to D9109)		
*2 M9110	Step transfer monitoring timer start (corresponds to D9110)		
*2 M9111	Step transfer monitoring timer start (corresponds to D9111)		
*2 M9112	Step transfer monitoring timer start (corresponds to D9112)		
*2 M9113	Step transfer monitoring timer start (corresponds to D9113)		
*2 M9114	Step transfer monitoring timer start (corresponds to D9114)		
M9180	Active step sampling trace completed flag	OFF: Trace start ON: Trace completed	• Turns ON when sampling trace of all designated blocks is completed. Turns OFF when sampling trace starts.
M9181	Active step sampling trace execution flag	OFF: Trace not executed ON: Trace executed	• Turns ON during sampling trace execution. Turns OFF at completion or suspension.
*2 M9182	Active step sampling trace enabled	OFF: Trace prohibit/suspend ON: Trace enabled	• Selects whether sampling trace execution is prohibited or enabled. ON: Sampling trace execution is enabled. OFF: Sampling trace execution is prohibited. When turned OFF during sampling trace execution, trace is suspended.
*2 M9196	Operation output at block stop	OFF: Coil output OFF ON: Coil output ON	• Selects the operation output state when block stop is executed. ON: The ON/OFF state of the coil used by the operation output of the step which was executed at block stop is retained. OFF: All coil outputs are turned OFF. (Operation output by a SET instruction is retained regardless of ON/OFF of M9196.)
M9197 M9198	Fuse blown/I/O verify error display switching	Switches display in combination of M9197 and M9198 status.	<table><tr><th>M9197</th><th>M9198</th><th>Display Range</th></tr><tr><td>OFF</td><td>OFF</td><td>Status of X/Y 0 to 7F0</td></tr><tr><td>ON</td><td>OFF</td><td>Status of X/Y 800 to FF0</td></tr><tr><td>OFF</td><td>ON</td><td>Status of X/Y 1000 to 17F0</td></tr><tr><td>ON</td><td>ON</td><td>Status of X/Y 1800 to 1FF0</td></tr></table>• Switches the I/O module number for the display of fuse-blown module (D9100 to D9107) and the display of I/O module verify check error (D9116 to D9123). • Display switching is executed at END processing.

Table 11.1 Special Relay List (Continued)

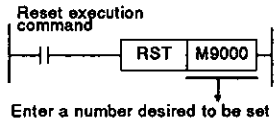
Number	Name	Description	Detailes
M9199	Online sampling trace/status latch data restore	OFF: Data restore not provided ON: Data restore provided	• When sampling trace/status latch is executed, set data stored in the CPU can be restored so the operation can be restarted. Turn ON M9199 when the execution is made again. (No need of rewriting data from peripherals.)

POINTS

(1) All special relays are switched off by any of the power-off, latch clear and reset operations. The special relays remain unchanged when the RUN/STOP switch is set to STOP.

(2) The above relays with numbers marked *1 remain "on" if normal status is restored. Therefore, to turn them "off", use the following method:

(a)Method by user program
Insert the circuit shown at the right into the program and turn on the reset execution command contact to clear the special relay M.



(b)Method by peripheral device
Cause forced reset by the text function of peripheral device.
For the operation procedure, refer to the manual of each peripheral device.

(c)By moving the RESET key switch at the CPU front to the RESET position, the special relay is turned "off".

(3) Special relays marked *2 are switched ON/OFF in the sequence program.

(4) Special relays marked *3 are switches ON/OFF in test mode of the peripheral.

(5) Items marked *4 are reset only when power is turned ON.

11.2 Special Register List

The special register are data registers used for specific purposes.

Therefore, do not write data to the registers in the program (except the ones with numbers marked *2 in the table).

Table 11.2 Special Register List

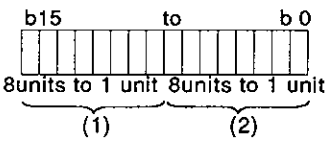
Number	Name	Stored Data	Explanation
D9000	Fuse blown	Fuse blow module number	• When fuse flow modules are detected, the lowest number of detected units is stored in hexadecimal. (Example: When fuses of Y50 to 6F output modules have blown, "50" is stored in hexadecimal) The module number monitored by the peripheral is hexadecimal. (Cleared when all contents of D9100 to D9107 are reset to 0.)
D9002	I/O unit verify error	I/O module verify error module number	• If I/O module data is different from data entered are detected when the power is turned on, ther first I/O number of the lowest number module among the detected modules stored in hexadecimal. (Storing method is the same as that of D9000.) The module number monitored by the peripheral is hexadecimal. (Cleared when all contents of D9116 of D9123 are reset to 0.)
*1 D9004	MINI link error	Stores the status of units (1 to 8) set in parameters	• Error occurrence detected by the MINI link master module is shown in bit pattern.  (1) Becomes "1" at MINI/MINI-S3 master station error occurrence (2) Becomes "1" if the AnUCPU and the master station of MINI(-S3) cannot be refreshed
*4 D9005	AC DOWN counter	AC DOWN time count	• 1 is added each time input voltage becomes 80% or less of rating while the CPU unit is performing operation, and the value is stored in BIN code.
*1 D9008	Self-diagnostic error	Self-diagnostic error number	• When error is found as a result of self-diagnosis, error number is stored in BIN code.
D9009	Annunciator detection	F number at which external failure has occurred	• When on of F0 to 2047 is turned on by [OUT F] or [SET F] the F number, which has been detected earliest among the F numbers which have turned on, is stored in BIN code. • D9009 can be cleared by [RST F] or [LEDR] instruction. If another F number has been detected, the clearing of D9009 causes the next number to be stored in D9009.
D9010	Error step	Step number at which operation error has occurred	• The module numbers of special function modules are stored if special function modules cannot be accessed when operation mode is changed from STOP to RUN. • When operation error has occurred during execution of application instruction, the step number, at which the error has occurred, is stored in BIN code. Thereafter, each time operation error occurs, the contents of D9010 are renewed.
D9011	Error step	Step number at which operation error has occurred	• When operation error has occurred during execution of application instruction, the step number, at which the error has occurred, is stored in BIN code. Since storage into D9011 is made when M9011 changes from off to on, the contents of D9010 cannot be renewed unless M9011 is cleared by user program.
D9014	I/O control mode	I/O control mode number	• The set mode is represented as follows: 3 = I/O in refresh mode

Table 11.2 Special Register List (Continued)

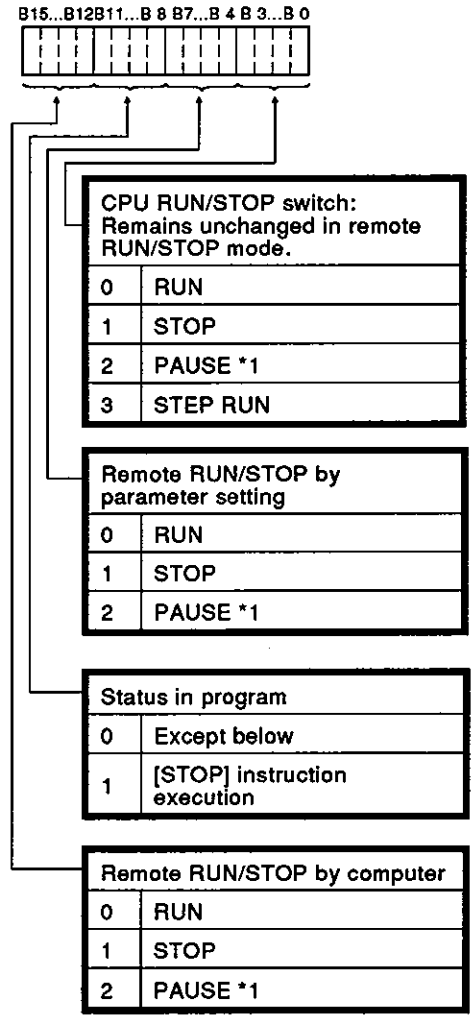
Number	Name	Stored Data	Explanation
D9015	CPU operating states	Operating states of CPU	• The operating states of CPU as shown below are stored in D9015.  *1 When the CPU is in RUN mode and M9040 is off, the CPU remains in RUN mode if changed to PAUSE mode.
D9016	Program number	The sequence program being executed is stored in BIN values.	• The sequence program currently executed is stored with the following code numbers: 0: ROM 1: RAM
D9017	Scan time	Minimum scan time (per 10 msec)	• If scan time is smaller than the content of D9017, the value is newly stored at each END. Namely, the minimum value of scan time is stored into D9017 in BIN code.
D9018	Scan time	Scan time (per 10 msec)	• Scan time is stored in BIN code at each END and always rewritten.
D9019	Scan time	Maximum scan time (per 10 msec)	• If scan time is larger than the content of D9019, the value is newly stored at each END. Namely, the maximum value of scan time is stored into D9019 in BIN code.
*2 D9020	Constant scan	Constant scan time (User specified in 10 msec increments)	• Sets user program execution intervals in 10 msec increments. 0: Constant scan function unused 1 to 20: Constant scan function used, program executes at intervals of (set value) X 10 msec.

Table 11.2 Special Register List (Continued)

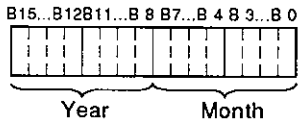
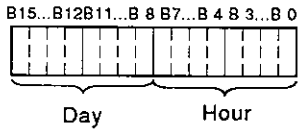
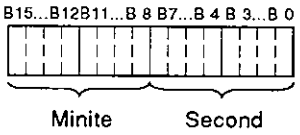
Number	Name	Stored Data	Explanation
D9021	Scan time	Scan time (1 msec units)	• Scan time is stored in BIN code at each END overwritting the present value.
D9022	Time	Time	• 1 is added every sec.
*2 D9025	Clock data	Clock data (Year, month)	• Stores the year (least significant digits) and month in BCD. Example: 1987, July → H8707 
*2 D9026	Clock data	Clock data (Day, hour)	• Stores the day and hour in BCD. Example: 31 st, 10 o'clock → H3110 
*2 D9027	Clock data	Clock data (Minute, second)	• Stores the minute and second in BCD. Example: 35 minutes, 48 seconds → H3548 

Table 11.2 Special Register List (Continued)

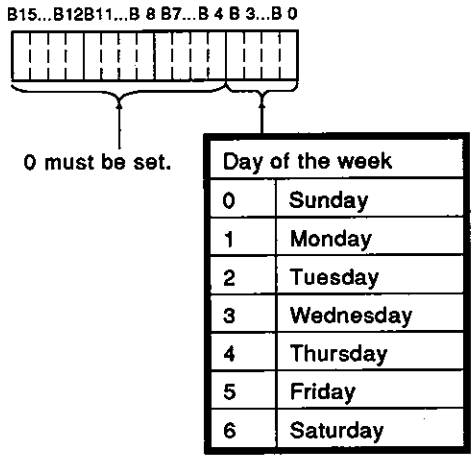
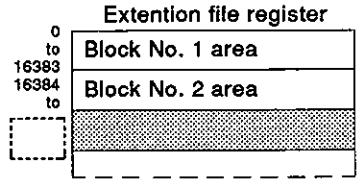
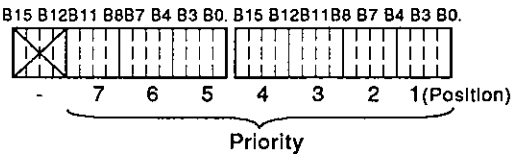
<table>
<tr><th>Number</th><th>Name</th><th>Stored Data</th><th>Explanation</th></tr>
<tr><td>*2
D9028</td><td>Clock data</td><td>Clock data (, day of the week)</td><td>• Stores the day of the week in BCD.
Example: Friday → H0005
 
</td></tr>
<tr><td>D9035</td><td>Extention file register</td><td>Used block number</td><td>• Currently used extension file register's block number is stored in BIN code.</td></tr>
<tr><td>D9036
D9037</td><td>For extention file register device number designation</td><td>Device numbers for direct access to each device of extension file registers</td><td>• Device numbers of extension file registers to which direct read or write is to be executed are designated in two-word binary data at D9036 and D9037. Device numbers are designated in continuous numbers beginning with R0 of block No. 1 regardless of block numbers.
 
</td></tr>
</table>

Table 11.2 Special Register List (Continued)

<table>
<tr><th>Number</th><th>Name</th><th>Stored Data</th><th>Explanation</th></tr>
<tr><td>*2
D9038</td><td rowspan="2">LED display priority</td><td>Priority 1 to 4</td><td rowspan="2">• Element number settings are changed to 1st to 4th (D9038) and 5th to 7th (D9039) display priority of the LED display in the CPU module.
 

<table><tr><th>Element No.</th><th>Content</th></tr><tr><td>0.</td><td>Not displayed</td></tr><tr><td>1.</td><td>I/O verify, fuse blown</td></tr><tr><td>2.</td><td>Special function module, link parameters, operation error</td></tr><tr><td>3.</td><td>CHK instruction error</td></tr><tr><td>4.</td><td>Annunciator</td></tr><tr><td>5.</td><td>LED instruction-related</td></tr><tr><td>6.</td><td>Battery error</td></tr><tr><td>7.</td><td>Clock data</td></tr></table>Even if "0" is set, errors due to which the CPU operations stop (including parameter settings) are unconditionally displayed on the LED.
Default value D9038 = H4321
D9039 = H0765</td></tr>
<tr><td>*2
D9039</td><td>Priority 5 to 7</td></tr>
<tr><td>D9044</td><td>For sampling trace</td><td>Step or time for sampling trace</td><td>• The value that D9044 contains is used as a sampling trace condition when the sampling trace instruction [STRA], [STRAR] is executed by switching ON/OFF M9044 from the peripheral device.
0 for scan
Time (in 10 msec increments) for time
The value is stored in BIN</td></tr>
<tr><td>D9049</td><td>SFC work area</td><td>Extention file register block number</td><td>• Extention file register block number used as the SFC work area is stored.
Higher 8 bits ..... Block number is stored.
Lower 8 bits ..... Step number is stored.</td></tr>
<tr><td>D9050</td><td>SFC program error code</td><td>Error code generated during SFC program execution</td><td>• Error codes generated during SFC program run are stored in BIN code.
0: No error
80: SFC program parameter error
81: Number of simultaneous execution steps exceeded
82: Block start error
83: SFC program operation error</td></tr>
<tr><td>D9051</td><td>Error block</td><td>Block number in which an error occurred</td><td>• Error brock numbers during SFC program run are stored in BIN code. In the case of error code 82, the start block number is stored.</td></tr>
<tr><td>D9052</td><td>Error step</td><td>Step number in which an error occurred</td><td>• Error step number in which error 83 occurred during SFC program run is stored in BIN code. In the case of error code 80 or 81, "0" is stored. In the case of error code 82, the block start step number is stored.</td></tr>
<tr><td>D9053</td><td>Error conversion</td><td>Conversion condition number with which an error occurred</td><td>• Error conversion condition number with which error 83 occurred during SFC program run is stored in BIN code. In the case of error code 80, 81 or 82. "0" is stored.</td></tr>
<tr><td>D9054</td><td>Error sequence step</td><td>Sequence step number with which an error occurred</td><td>• The sequence step number of conversion condition and operation output when error 83 occurred during SFC program run is stored in BIN code</td></tr>
<tr><td>D9055</td><td>Status latch</td><td>Status latch step</td><td>• The step number executed when the status is latched is stored in BIN code.</td></tr>
</table>

Table 11.2 Special Register List (Continued)

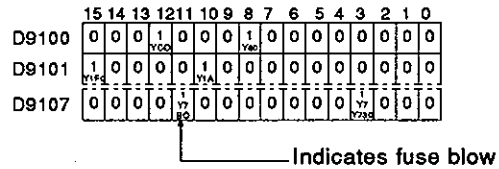
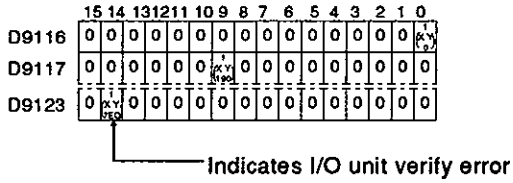
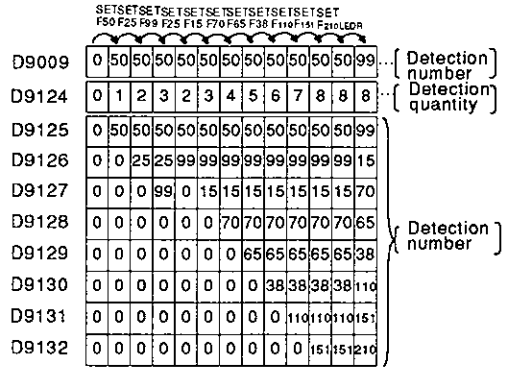
Number	Name	Stored Data	Explanation
D9072	PC communication check	Computer link data check	• Used at self-loopback check
D9081	Empty communication request entry areas	Empty communication request entry areas	• The quantity of empty areas of communication request entry areas, which can be entered, to MNET/MINI(-S3) is stored. (Max. 32)
*1 D9090	Excessive special function modules	Excessive special function modules	• When the number of special function modules loaded is excessive, the value of the "(head I/O number of the last special function module to be entered) ÷ 16" is stored as a BIN value.
*1 D9091	Detailed error numbers	Self-diagnostic detailed error numbers	• The detailed error number when a self-diagnostic error occurs is stored.
D9100 D9101 D9102 D9104 D9105 D9106 D9107	Fuse blown module	Bit pattern in modules of 16 points of fuse blow modules	• Output module numbers (in units of 16 point), of which fuses have blown, are enterd in bit pattern. (Preset output number when patameter setting has been performed.) • The blown fuse status of a remote station's output unit can be detected.  • By switching ON/OFF M9197 and M9198, the I/O module number display range is switched. • To clear data of a fuse-blown module, turn OFF M9000 (fuse blown).
D9116 D9117 D9118 D9119 D9120 D9121 D9122 D9123	I/O module verify error	Bit pattern n modules of 16 points of verify error modules	• When I/O module data is different from those entered at have been detected, the I/O module numbers (in units of 16 points) are entered in bit pattern. (Preset I/O module numbers when patameter setting has been performed.)  • By switching ON/OFF M9197 and M9198, the I/O module number display range is switched. • Data of a fuse-blown module is cleared by turning OFF M9000 (fuse blown).
D9124	Annunciator detection quantity	Annunciator detection quantity	• When one of F0 to 2047 is turned ON by [OUT F] or [SET F], 1 is added to the contents of D9124. When [RST F] or [LED R] instruct is executed, 1 is subtructed from the contents of D9124. • Quantity, which has been turned ON by [OUT F] or [SET F] is stored into D9124 in BIN code. The value of D9124 is maximum 8.

Table 11.2 Special Register List (Continued)

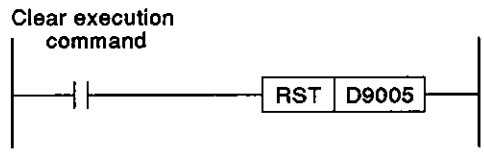
Number	Name	Stored Data	Explanation
D9125 D9126 D9127 D9128 D9129 D9130 D9131 D9132	Annunciator detection number	Annunciator detection number	• When one of F0 to 2047 is turned ON by [OUT F] or [SET F], F number, which has turned ON, is entered into D9125 to D9132 in due order in BIN code. • F number, which has been turned OFF by [RST F], is erased from D9125 to D9132, and the contents of data registers succeeding the data register, where the erased F number was stored, are shifted to the preceding data registers. • By executing [LED R] instruction, the contents of D9125 to D9132 are shifted upward by one. • When there are 8 annunciator detections, the 9th one is not stored into D9125 to D9132 even if detected. 

POINTS

(1) All special register data is cleared by any of the power-off, latch clear and reset operations. The data is retained when the RUN/STOP switch is set to STOP.

(2) For the above special registers with numbers marked *1, the contents of register are not cleared if normal status is restored. Therefore, to clear the contents, use the following method:

(a) Method by user program.
Insert the circuit shown at right into the program and turn on the clear execution command contact to clear the contents of register.



(b) Method by peripheral device.
Set the register to "0" by changing the present value by the test function of peripheral device or set to "0" by forced reset. For the operation procedure, refer to the manual of each peripheral device.

(c) By moving the RESET key switch at the CPU front to the RESET position, the special register is set to "0".

(3) For items marked *2, data is written in the sequence program.

(4) For items marked *3, data is written in the test mode of peripheral devices.

(5) For items marked *4, data is cleared the powers is turned ON.

11.3 Instruction List

Instructions used with the A2ASCPU are listed below.
Refer to the following programming manuals for details of the instructions.

- ACPU Programming Manual (Fundamentals)
- ACPU Programming Manual (Common Instructions)
- AnACPU Programming Manual (Dedicated Instructions)
- AnACPU Programming Manual (AD57 Instructions)
- AnACPU Programming Manual (PID Control Instructions)

(1) Sequence instructions

(a) Contact instruction

Contact	LD, LDI, AND, ANI, OR, ORI

(b) Connection instruction

Connection	ANB , ORB, MPS, MRD, MPP

(c) Output instruction

Output	OUT, SET, RST, PLS, PLF

(d) Shift instruction

Shift	SFT, SFTP

(e) Master control instruction

Master control	MC, MCR

(f) Termination instruction

Program end	FEND, END

(g) Other instructions

Stop	STOP
No operation	NOP
Page feed (page feed operation of printer output)	NOPLF

(2) Basic instructions

(a) Comparison instructions

=	16 bits	LD=, AND=, OR=
	32 bits	LDD=, ANDD=, ORD=
< >	16 bits	LD<>, AND<>, OR<>
	32 bits	LDD<>, ANDD<>, ORD<>
>	16 bits	LD>, AND>, OR>
	32 bits	LDD>, ANDD>, ORD>
≤	16 bits	LD<=, AND<=, OR<=
	32 bits	LDD<=, ANDD<=, ORD<=
<	16 bits	LD<, AND<, OR<
	32 bits	LDD<, ANDD<, ORD<
≥	16 bits	LD>=, AND>=, OR>=
	32 bits	LDD>=, ANDD>=, ORD>=

(b) BIN arithmetic operation instruction

+ Addition	16 bits	Two types each for + and +P
	32 bits	Two types each for D+ and D+P
- Subtraction	16 bits	Two types each for - and -P
	32 bits	Two types each for D- and D-P
* Multiplication	16 bits	*, *P
	32 bits	D*, D*P
/ Division	16 bits	/, /P
	32 bits	D/, D/P
+1 Addition	16 bits	INC, INCP
	32 bits	DINC, DINCP
-1 Subtraction	16 bits	DEC, DECP
	32 bits	DDEC, DDECP

(c) BCD arithmetic operation instructions

+ Addition	BCD 4 digits	Two types each for B+ and B+P
	BCD 8 digits	Two types each for DB+ and DB+P
- Subtraction	BCD 4 digits	Two types each for B- and B-P
	BCD 8 digits	Two types each for DB-P and DB-P
* Multiplication	BCD 4 digits	B*, B*P
	BCD 8 digits	DB*, DB*P
/ Division	BCD 4 digits	B/, B/P
	BCD 8 digits	DB/, DB/P

(d) BCD - BIN conversion instructions

BIN→BCD	16 bits	BCD, BCDP
	32 bits	DBCD, DBCDP
BCD→BIN	16 bits	BIN, BINP
	32 bits	DBIN, DBINP

(e) Data transfer instructions

Transfer	16 bits	MOV, MOVP
	32 bits	DMOV, DMOVP
Change	16 bits	XCH, XCHP
	32 bits	DXCH, DXCHP
Undefined transfer	16 bits	CML, CMLP
	32 bits	DCML, DCMLP
Block transfer	16 bits	BMOV, BMOVP
Repeat data block transfer	16 bits	FMOV, FMOVP

(f) Program branch instructions

Jump	CJ, SCJ, FMP
Subroutine call	CALL, CALLP, RET
Interrupt program enable/disable	EI, DI, IRET

(g) Refresh instructions

Link refresh	COM
Partial refresh	SEG

(3) Application instructions

(a) Logical operation instruction

Logical product	16 bits	Two types each for WAND and WANDP
	32 bits	DAND, DANDP
Logical sum	16 bits	Two types each for WOR and WORP
	32 bits	DOR, DORP
Exclusive logical sum	16 bits	Two types each for WXOR and WXORP
	32 bits	DXOR, DXORP
NOT exclusive logical sum	16 bits	Two types each for WXNR and WXNRP
	32 bits	DXNR, DXNRP
2's complement (reversed sign)	16 bits	NEG, NEGP

(b) Rotation instructions

Right ward rotation	16 bits	ROR, RORP, RCR, RCRP
	32 bits	DROR, DRORP, DRCR, DRCRP
Left ward rotation	16 bits	ROL, ROLP, RCL, RCLP
	32 bits	DROL, DROLP, DRCL, DRCLP

(c) Shift instructions

Right ward shift	16 bits	SFR, SFRP, BSFR, BSFRP
	Per device	DSFR, DSFRP
Left ward shift	16 bits	SFL, SFLP, BSFL, BSFLP
	Per device	DSFL, DSFLP

(d) Data processing instruction

Data search	16 bits	SER, SERP
Bit check	16 bits	SUM, SUMP
	32 bits	DSUM, DSUMP
Decode	2^n bits	DECO, DECOP
	16 bits	SEG
Encode	2^n bits	ENCO, ENCOP
Bit set	16 bits	BSET, BSETP
Bit reset	16 bits	BRST, BRSTP
Dissociation	16 bits	DIS, DISP
Association	16 bits	UNI, UNIP

(e) FIFO instructions

Write	16 bits	FIFW, FIFWP
Read	16 bits	FIFR, FIFRP

(f) ASCII instructions

ASCII conversion	ASC
ASCII print	Two types each for PR and PRC

(g) Buffer memory access instructions

Data read	1 word	FROM, FROMP
	2 words	DFRO, DFROP
Data write	1 word	TO, TOP
	2 words	DTO, DTOP

(h) FOR NEXT instruction

Repetition	FOR, NEXT

(i) Display instructions

Display	LED, DEDC
Display reset	LEDR

(j) Data link unit instructions

Data read	1 word	LRDP, RFRP
Data write	1 word	LWTP, RTOP

(k) Other instructions

WDT reset		WDT, WDTP
Fault check		CHK
Status latch		SLT, SLTR
Sampling trace		STRA, STRAR
Carry flag set/reset	1 bit	STC, CLC
Timing clock	1 bit	DUTY

(4) Dedicated instructions

(a) Direct processing instructions

Direct output	DOUT
Direct set	DSET
Direct reset	DRST

(b) Instructions for structured program

Circuit index qualification	IX, IXEND
Repeat forced end	BREAK
Subroutine call	FCALL
Changes in error check circuit pattern	CHK, CHKEND

(c) Data operation instructions

32-bit data search	DSER
16-bit upper and lower byte exchange	SWAP
Separation of data	DIS
Association of data	UNI
Bit test	TEST, DTEST

(d) I/O operation instructions

Flip-flop control	FF
Numerical key input from keyboard	KEY

(e) Real number processing instructions (BCD real number processing instructions)

The square root calculation of BCD 4 digits	BSQR
The square root calculation of BCD 8 digits	BDSQR
SIN (sine) operation	BSIN
COS (cosine) operation	BCOS
TAN (tangent) operation	BTAN
SIN^{-1} (arcsine) operation	BASIN
COS^{-1} (arccosine) operation	BACOS
TAN-1 (arctangent) operation	BATAN

(f) Real number processing instructions (Floating point real number processing)

Real numbers to 16-/32-bit BIN conversion	INT, DINT
16-/32-bit BIN to real numbers conversion	FLOAT, DFLOAT
Addition	ADD
Subtraction	SUB
Multiplication	MUL
Division	DIV
Angle to radian conversion	RAD
Radian to angle conversion	DEG
SIN (sine) operation	BSIN
COS (cosine) operation	BCOS
TAN (tangent) operation	BTAN
SIN-1 (arcsine) operation	BASIN
COS-1 (arccosine) operation	BACOS
TAN-1 (arctangent) operation	BATAN
Square root	SQR
Exponent	EXP
Logarithm	LOG

(g) Character string processing instructions

16-/32-bit BIN to decimal ASCII conversion	BINDA, DBINDA
16-/32-bit BIN to hexadecimal ASCII conversion	BANHA, DBINHA
16-/32-bit BCD to decimal ASCII conversion	BCDDA, DBCDDA
Decimal ASCII to 16-/32-bit BIN conversion	DABIN, DDABIN
Hexadecimal ASCII to 16-/32-bit BIN conversion	HABIN, DHABIN
Decimal ASCII to 16-/32-bit BCD conversion	DABCD, DDABCD
Device comment read	COMRD
Character string length detection	LEN
16-/32-bit BIN to decimal character string conversion	STR, DSTR
Decimal character string to 16-/32-bit BIN conversion	VAL, DVAL
Hexadecimal data to ASCII conversion	ASC
ASCII to hexadecimal data conversion	HEX
Character string transfer	SMOV
Character string association	SADD
Character string comparison	SCMP
Separation into units of 1 byte	WTOB
Combination into units of 1 byte	BTOW

(h) Data control instructions

Upper/lower limit control	LIMIT, DLIMIT
Dead zone control	BAND, DBAND
Zone control	ZONE, DZONE

(i) Clock instructions

Clock data read	DATERD
Clock data write	DATEWR

(j) Extension file register instructions

Block number change of extension file register	RSET
Block move of extension file register	BMOVR
Block exchange of extension file register	BXCHR
Direct read in units of 1 word of extension file register	ZRRD
Direct read in units of 1 byte of extension file register	ZRRDB
Direct write in units of 1 word of extension file register	ZRWR
Direct write in units of 1 byte of extension file register	ZRWRB

(k) Data link instructions

Reading word device data from local stations	LRDP
Writing data to word devices in local stations	LWTP
Reading data from remote I/O station special function modules	RFRP
Writing data to remote I/O station special function modules	RTOP

(l) AD61(S1) high speed counter module control instructions

Preset value data setting	PVWR1, PVWR2
Set value data write for comparison and coincidence identification	SVWR1, SVWR2
Present value read from CH1/CH2	PVRD1, PVRD2

*: These instructions cannot be used for A1SD61.

(m) AJ71C24(S8) computer link module control instructions

Data send	Characters up to 00H code	PR
	Designated number of characters	PRN
Data receive		INPUT
Communication status read		SPBUSY
Communication processing forced stop		SPCLR

(n) AJ71C21(S1) terminal interface module control instructions

Data output to RS-232C (data up to 00H code)	PR2
Data output to RS-422 (data up to 00H code)	PR4
Data output to RS-232C (designated number of points)	PRN2
Data output to RS-422 (designated number of points)	PRN4
Data read and input through RS-232C	INPUT2
Data input from RS-422	INPUT4
Read from the RAM memory	GET
Write to the RAM memory	PUT
Communication status read	SPBUSY
Communication processing forced stop	SPCLR

(o) AJ71PT32-S3 MELSECNET/MINI-S3 master module control instructions

Key input from operation box	INPUT
Data send/receive of specified number of bytes to and from the AJ35PTF-R2	PR, PRN, INPUT
MINI standard protocol module data read/write	MINI
Error reset for the remote terminal module	MINIERR
Communication status read	SPBUSY
Communication processing forced stop	SPCLR

(p) PID instructions

Control data setting	PIDINIT
PID operations	PIDCONT
Monitoring PID operation results at AD57(S1)	PID57

*1: Newly created dedicated instructions for AnUCPU

(q) AD59(S1) memory card/centronics interface module control instructions

Output to printer	Characters up to 00H code	PR
	Designated number of characters	PRN
Data read from memory card		GET
Data write to memory card		PUT

(r) AD57(S1)/AD58 control instructions

Display mode setting instruction		CMODE
Screen display control instruction	Canvas screen display	CPS1
	VRAM display address change	CPS2
	Canvas transfer	CMOV
	Screen clear	CLS
	VRAM clear	CLV
	Scroll up/down	CSCRU, CSCRD
Cursor control instructions	Cursor display	CON1, CON2
	Cursor delete	COFF
	Cursor setting	LOCATE
Display condition setting instructions	Forward/reverse rotation of characters to be displayed	CNOR, CREV
	Forward/reverse rotation switching of characters	CRDSP, CRDSPV
	Character color specification	COLOR
	Character color change	CCDSP, CCDSPV
Specified character display instructions	ASCII character display	PR, PRN
	ASCII character write	PRV, PRNV
	Character display	EPR, EPRN
	Character write	EPRV, EPRNV
	Repetitive display of same characters	CR1, CR2, CC1, CC2
Fixed character display instructions	Minus display	CINMP
	Hyphen display	CINHP
	Period (decimal) display	CINPT
	Numeral display	CIN0 to CIN9
	English alphabet display	CINA to CINZ
	Space display	CINSP
Specified column clear instruction		CINCLR
ASCII code conversion instructions of display character string		INPUT
VRAM data control instructions	VRAM data read	GET
	VRAM data write	PUT
Display condition read instruction		STAT

APPENDICES

APPENDIX 1 PERIPHERAL DEVICES

(1) Compatibility of peripheral devices and system FDs which have been used with existing systems is as given in the table below.

Peripheral Device Name	Software Package Name	Compatibility	Usable Range	PC Type Set at Start Up
A6GPP/A6PHP	SW4GP-GPPAEE	Usable	Within the device range of A2ACPU(S1)	A2A
	SW3GP-GPPAEE	Usable	Within the device range of A3HCPU	A3H
	Before SW2[ ][ ] type	Unusable	———	———
A6HGP	SW3-HGPA	Usable	Within the device range of A3HCPU	A3H
	Before SW2[ ][ ] type	Unusable	———	———
PC/AT (IBM)	SW0IX-GPPAE MELSEC-MEDOC	Usable	Within the device range of A2ACPU(S1)	A2A
A8PUE	———	Usable	Within the device range of A2ACPU(S1)	———
A7PU A7PUS	———	Usable	Within the device range of A3HCPU	———
A6WU	• A6WU which has an "E" mark on the name plate.	Usable	Within the device range of A3HCPU	———
	• A6WU which does not have an "D" mark on the name plate.	Unusable	———	———

APPENDIX 2 PRECAUTIONS FOR USING EXISTING SEQUENCE PROGRAMS WITH THE A2ASCPU

Described below are the precautions for using sequence programs prepared for the A1SCPU with the A2ASCPU.

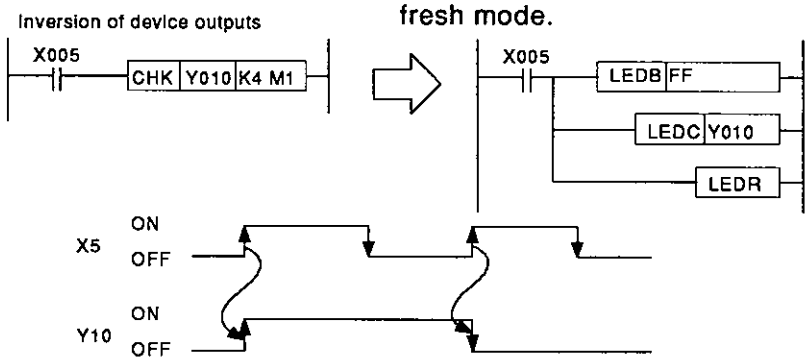
POINT

All sequence programs for the A1SCPU are compatible with the A2ASCPU.

2.1 Instructions of Different Specifications

This section describes how to change a sequence program to use instructions of different specifications. Instructions not included herein basically need not be changed.

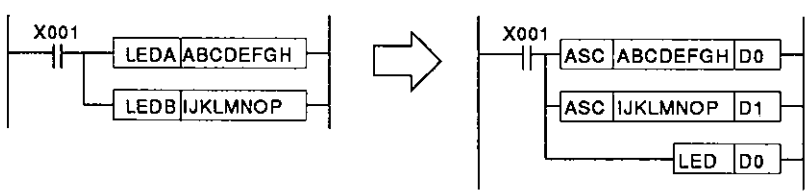
(1) CHK instruction ..... This instruction must be changed when the A1SCPU is to be used in the refresh mode.



(2) DI/EI instructions ..... These instructions must be changed when the special relay M9053 is turned ON.

- When the M9053 is ON, link refresh is enabled (EI) or disabled (DI).
- The A2ASCPU cannot enable or disable link refresh while a sequence program is being executed, because link refresh is performed by END processing.
  Correct the sequence program.

(3) LEDA/LEDB instructions



(4) SUB and SUBP instructions ..... Incompatible with the A2ASCPU.

- Since the A2ASCPU cannot store microcomputer programs, the SUB instruction cannot be used.

2.2 Special Relays and Special Registers of Different Specifications

The A2ASCPU cannot use the following special relays and special register. The relays and register in the program to be used with the A2ASCPU do not cause errors (they will be ignored), however, it is advisable to delete them from the program.

- M9010 .....Turned ON when an operation error occurs during execution, and turned OFF when the error is eliminated.
- M9053 .....Enables the EI instruction for link refresh/interrupt program, and disables the DI instruction for link refresh/interrupt program.
- D9010 .....Stores the step number at which an error has occurred. (The step number will be updated every time an error occurs.)

2.3 Parameter Setting

The parameters, whose settings are stored in the existing CPU, can be used without any change, if they are not as described below.

Setting Item	Description
Microcomputer program capacity	The microcomputer program area of the A2ASCPU is dedicated to the SFC. If a microcomputer program utility package is stored in the microcomputer program area of the existing CPU, a "parameter error" occurs.
Module type registration by I/O allocation	When the existing system uses an AD57, an AD57-S1 and an AD58, a SW[ ]-AD57P utility package is stored in the microcomputer program area. Because the A2ASCPU has no microcomputer program area, it cannot store the utility package. To make use of this utility package function, the A2ASCPU incorporates a dedicated instruction for special function modules. Before using this A2ASCPU's dedicated instruction, the modules must be registered in their module types by parameter I/O allocation.

The following parameters are not processed according to the settings in the existing CPU.

- Watchdog timer setting .... The set time is ignored, and this parameter is treated as 200 msec.
- Interrupt counter setting ... The interrupt counter set in the A1SCPU is ignored, and the interrupt counter is treated as a normal one on the sequence program.

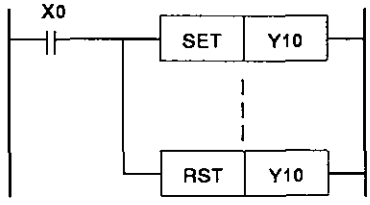
2.4 I/O Control System

For the I/O control system, the A2ASCPU adopts the refresh mode (partial direct I/O according to instructions), which is different from that for the A1SCPU. Consequently, the input (X) read timing and the output (Y) transmission timing to external devices are different between the two CPUs.

(1) Pulse processing program on SET/RST instructions

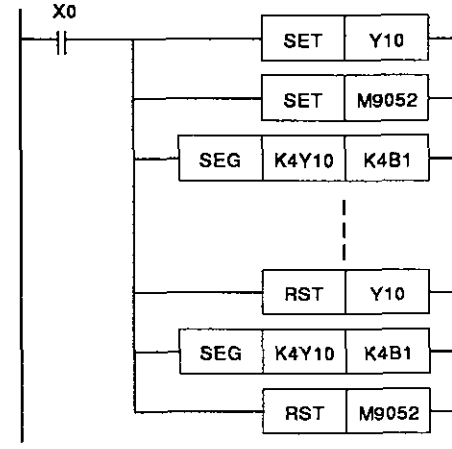
Use the following program to allow the A2ASCPU to execute pulse output to external devices on the SET/RST instructions processed by the A1SCPU in the direct mode.

A1SCPU direct mode

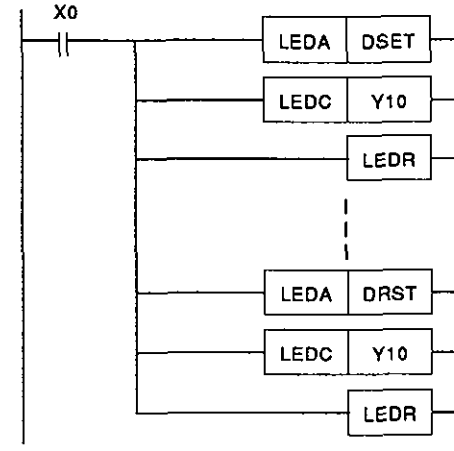


(a) When using instructions common to ACPUs

A2ASCPU



(b) When using dedicated instructions for the A2ASCPU



POINT

Also when a special function module, such as the AD61 (S1) high speed counter module, is mounted, use the above program to give out pulse signals to it.

2.5 Microcomputer Programs

Since the A2ASCPU adopts no microcomputer mode, it cannot use the utility software packages and user-prepared microcomputer programs used for the A1SCPU. (The microcomputer program area of the A2ASCPU is exclusively allocated to the SFC.)
When the above software packages and microcomputer programs are used, delete all the SUB instructions (microcomputer program calls) to execute them from the sequence program.
To use the utility packages listed below, change them into programs based on dedicated instructions for the A2ASCPU.

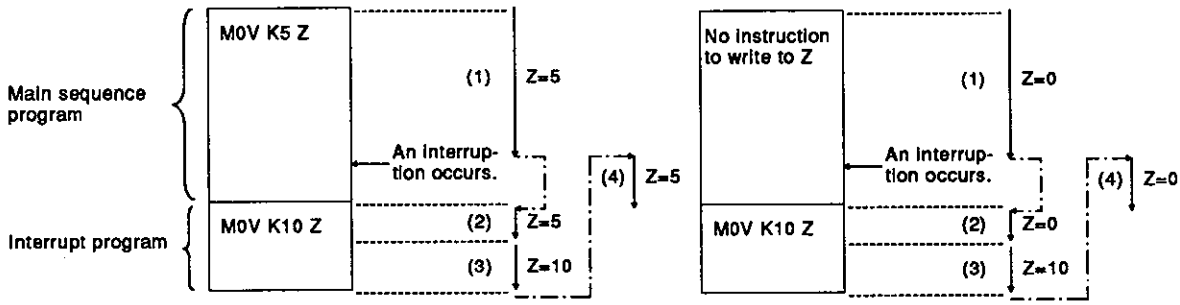
(1) SW[ ]-AD57P ..... AnACPU Programming Manual (AD57)
(usable for creating campus
and character generators)

(2) SW[ ]-UTLP-FN0 ..... AnACPU Programming Manual (Dedicated Instructions)

(3) SW[ ]-UTLP-PID ..... AnACPU Programming Manual (PID)

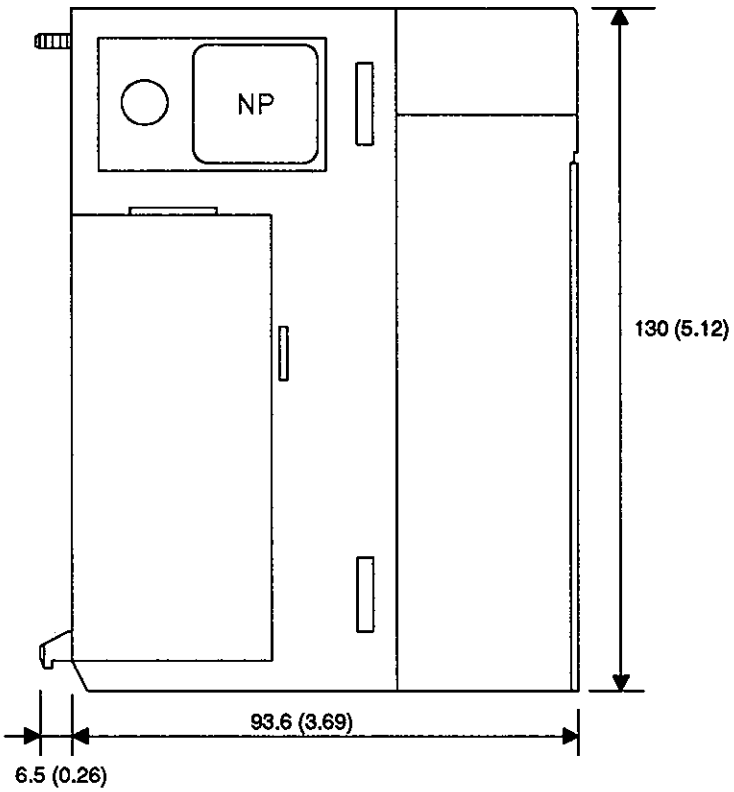
2.6 Index Register Processing

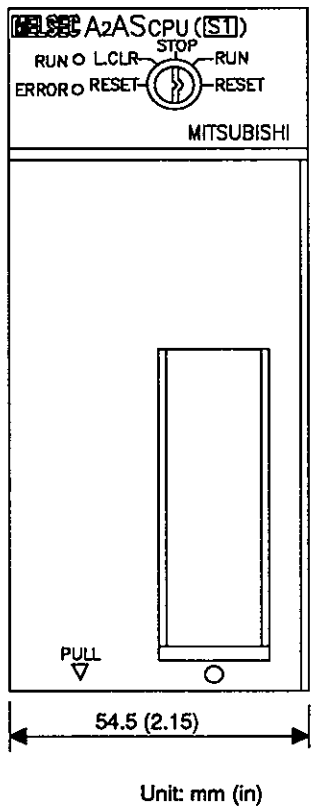
Even if they are updated while an interrupt program is being executed, the index registers in the A2ASCPU will return to the values before executing the interrupt program when processing proceeds to the main or sequence program.



APPENDIX 3 OUTSIDE DIMENSIONS

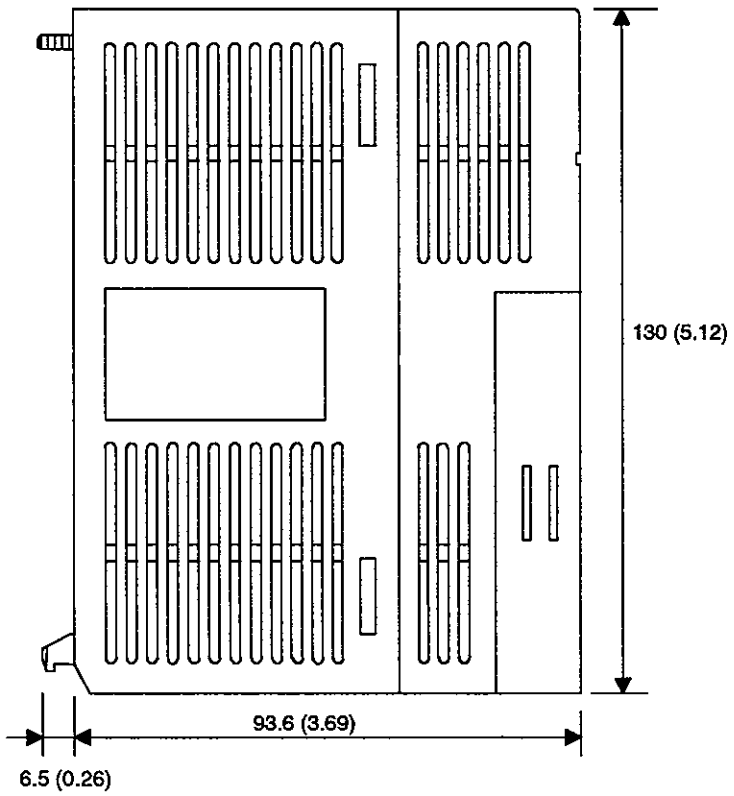
3.1 A2ASCPU(S1) Module

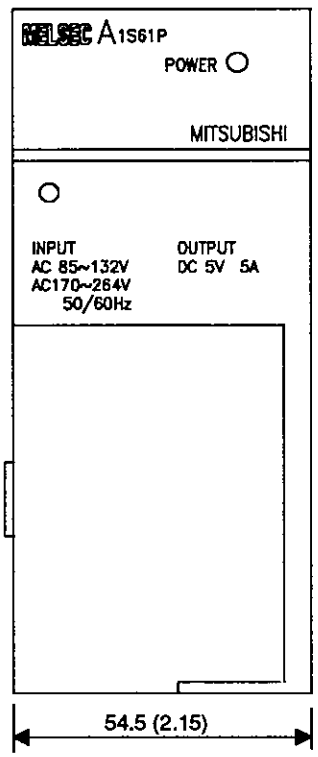




Unit: mm (in)

3.2 A1S61P/A1S62P/A1S63P Power Supply Module

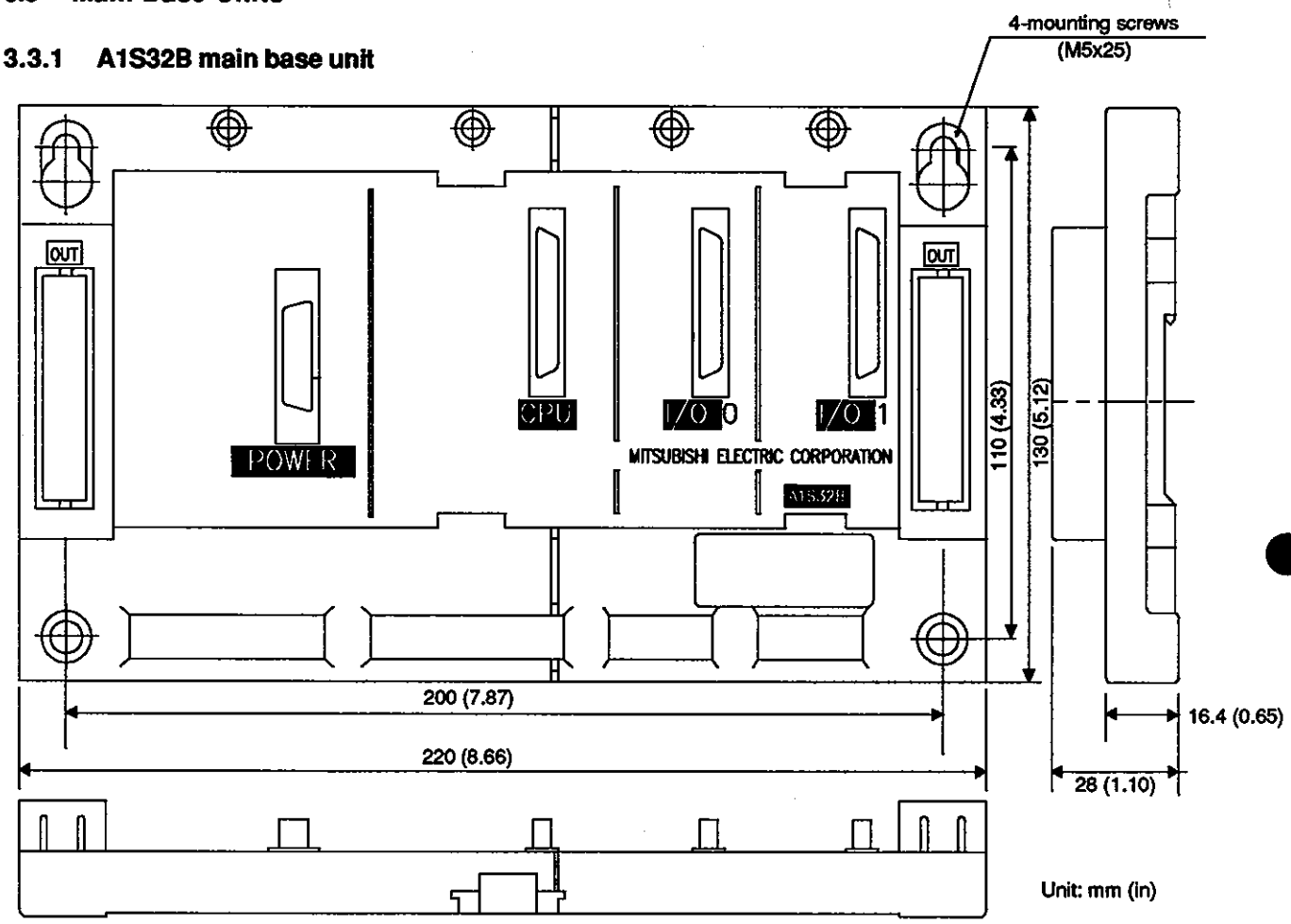




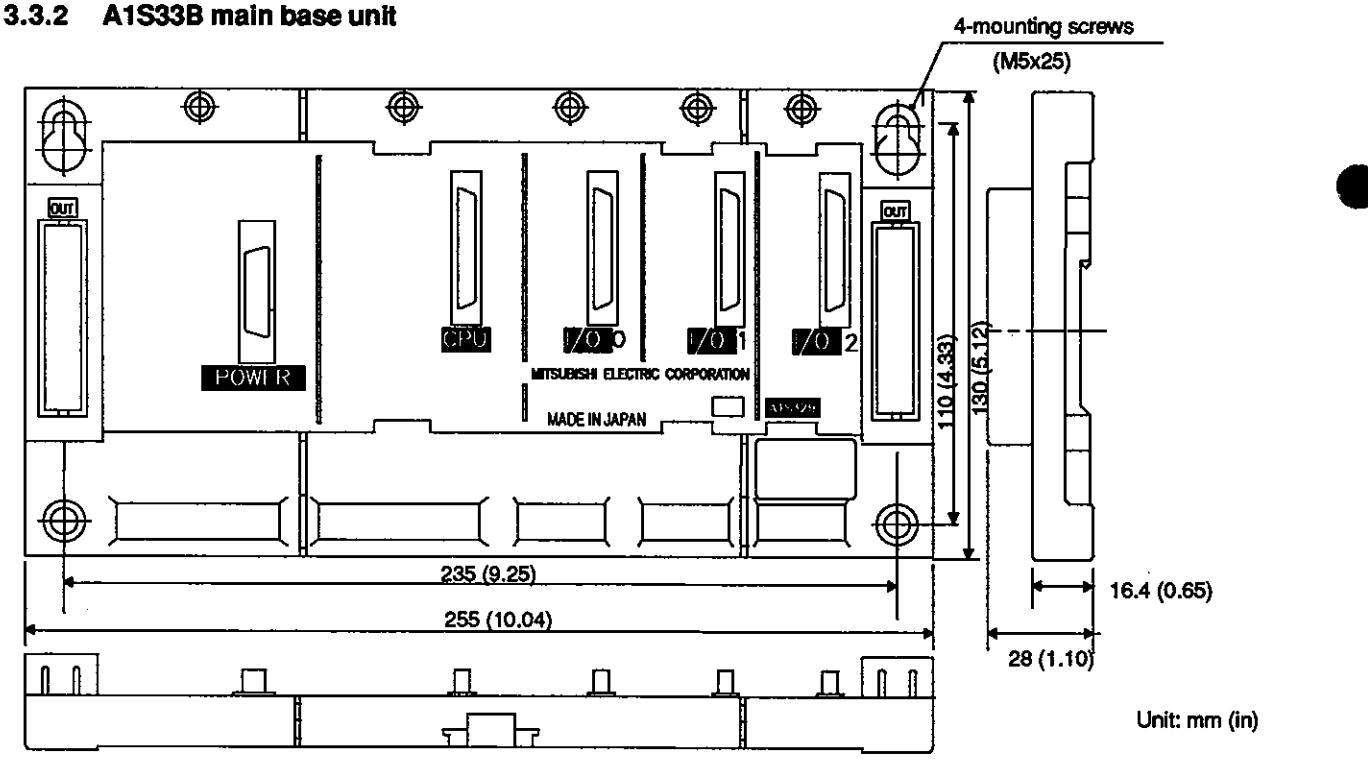
Unit: mm (in)

3.3 Main Base Units

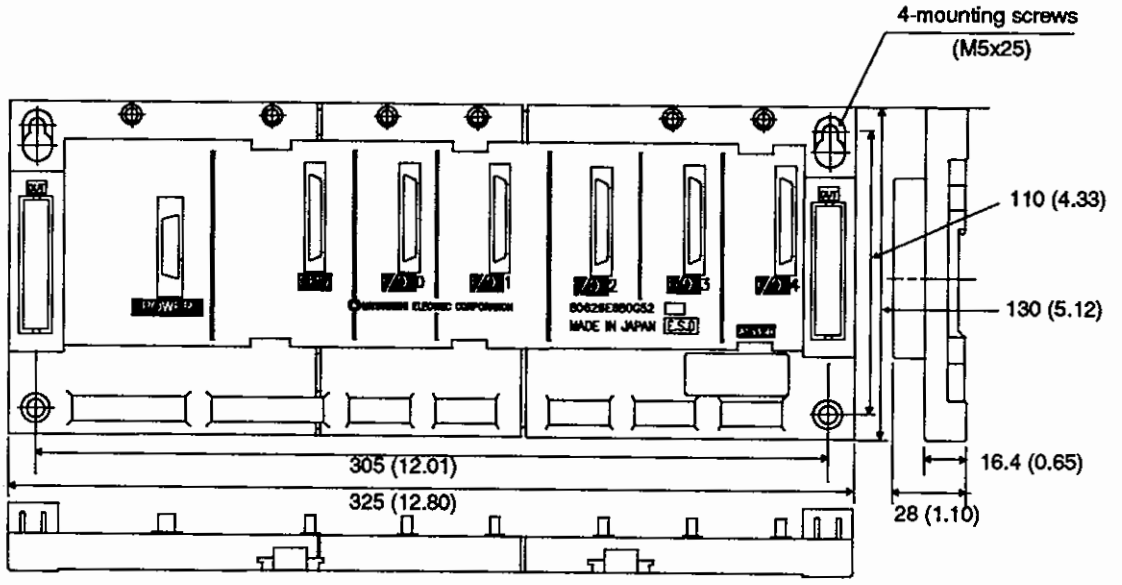
3.3.1 A1S32B main base unit



3.3.2 A1S33B main base unit

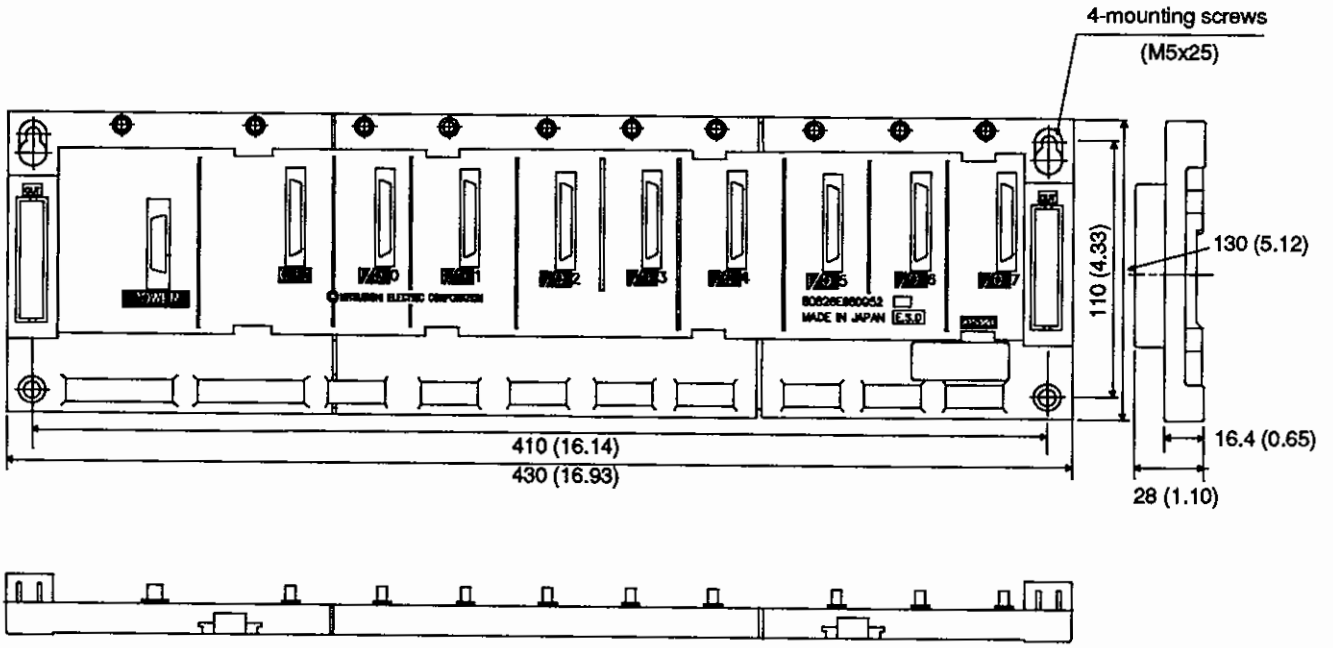


3.3.3 A1S35B main base unit



Unit: mm (in)

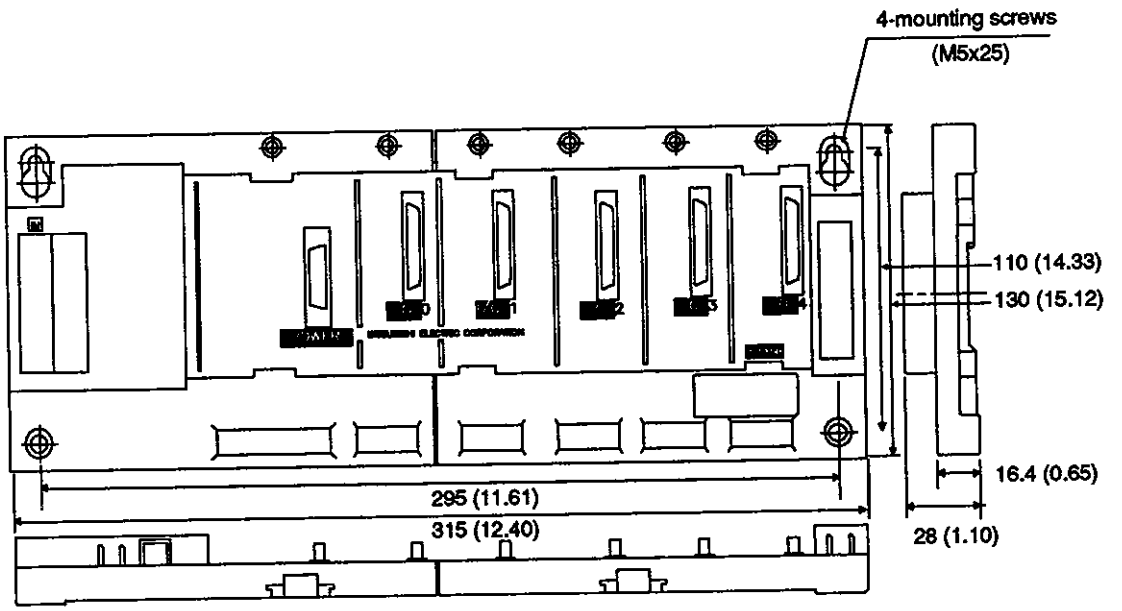
3.3.4 A1S38B main base unit



Unit: mm (in)

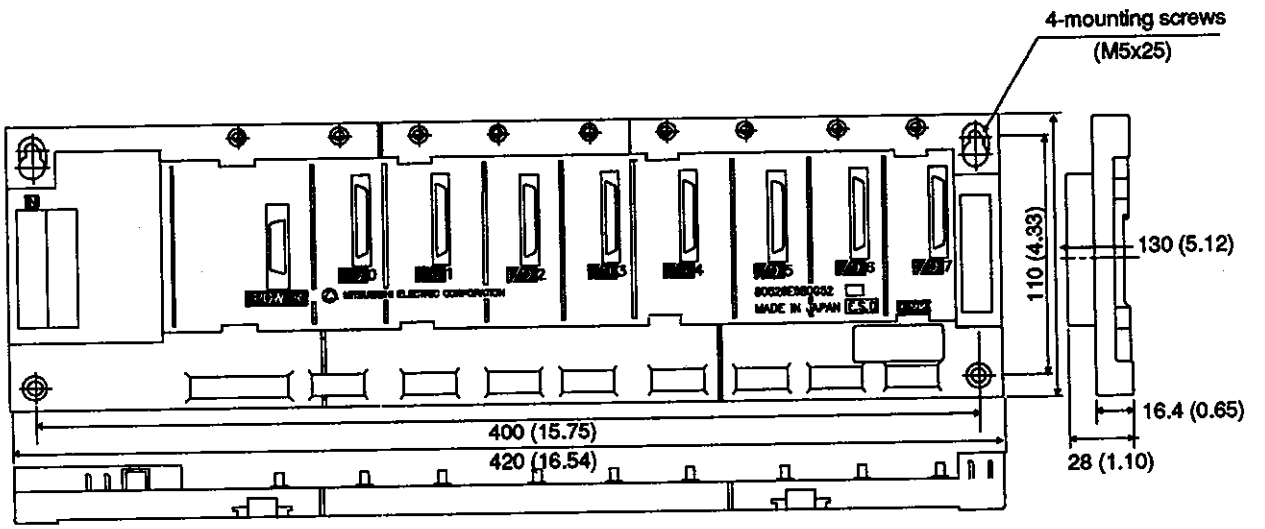
3.4 Extension Base Units

3.4.1 A1S65B extension base unit



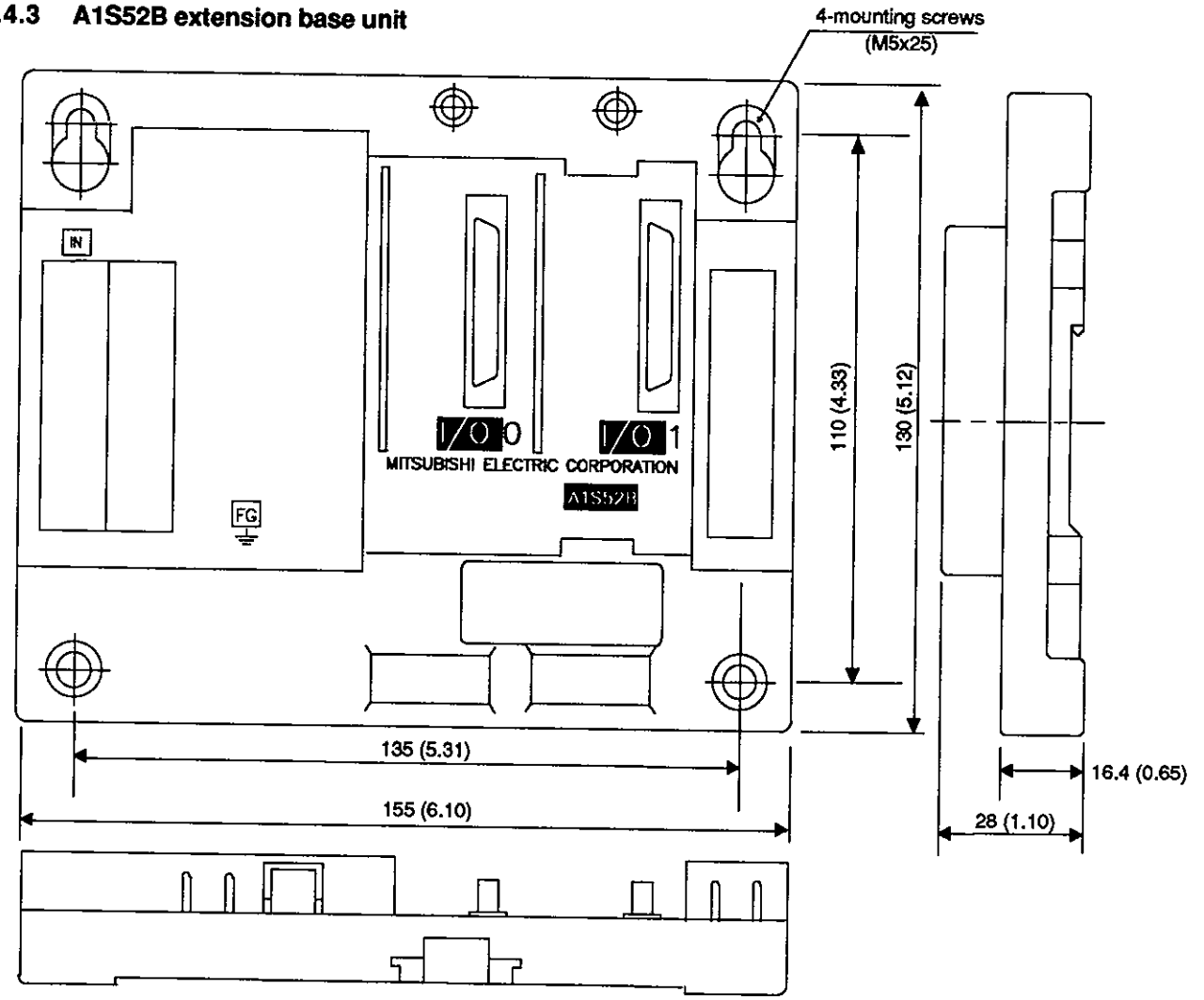
Unit: mm (in)

3.4.2 A1S68B extension base unit



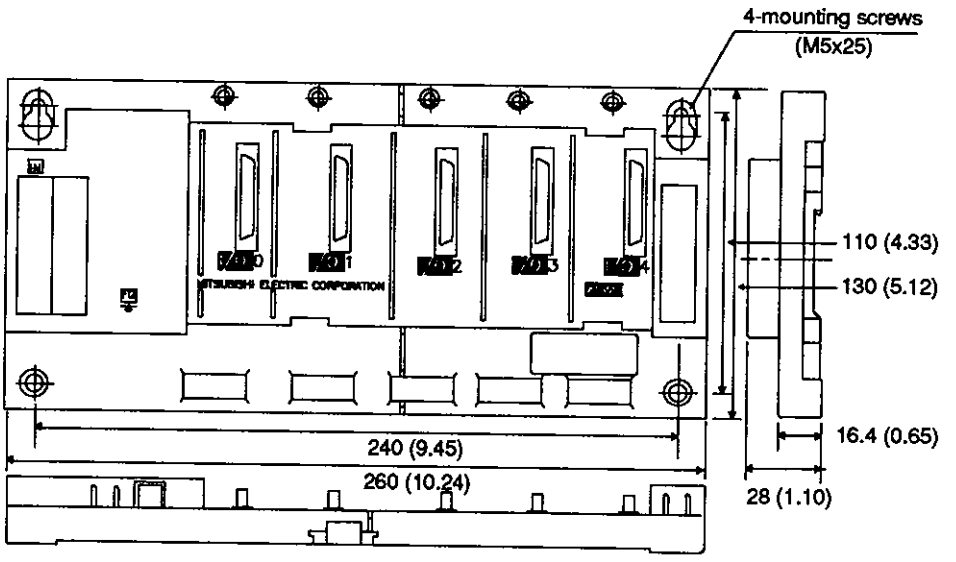
Unit: mm (in)

3.4.3 A1S52B extension base unit



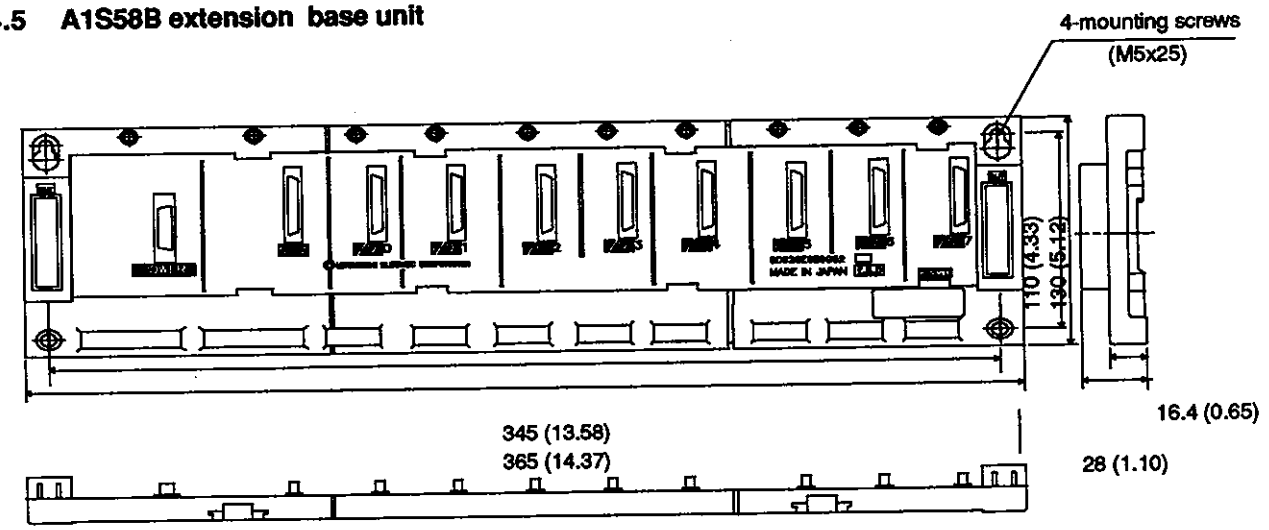
Unit: mm (in)

3.4.4 A1S55B extension base unit



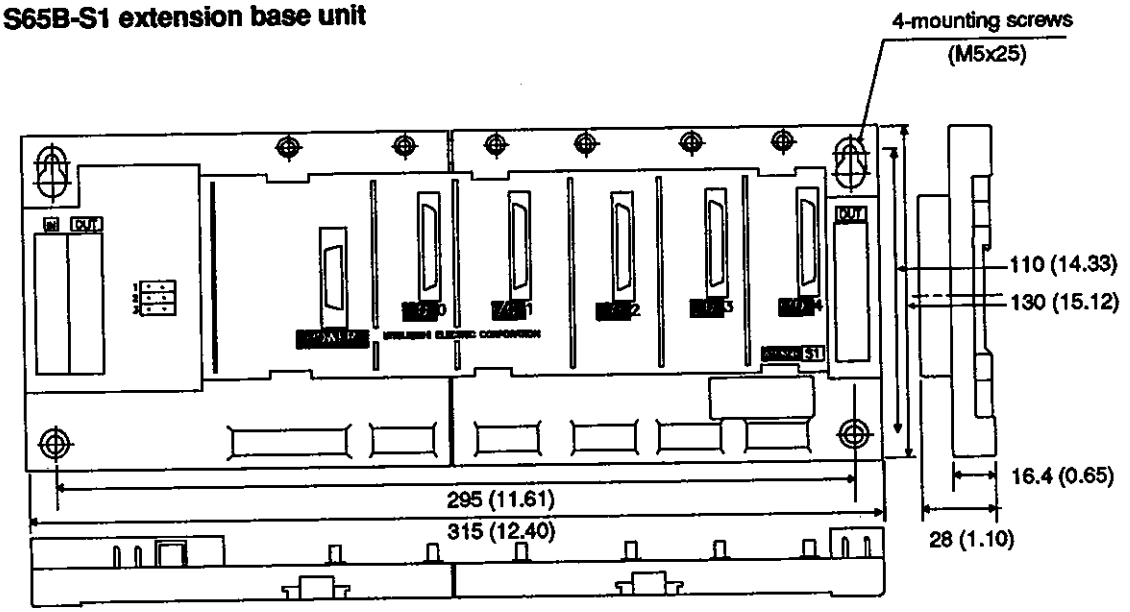
Unit: mm (in)

3.4.5 A1S58B extension base unit



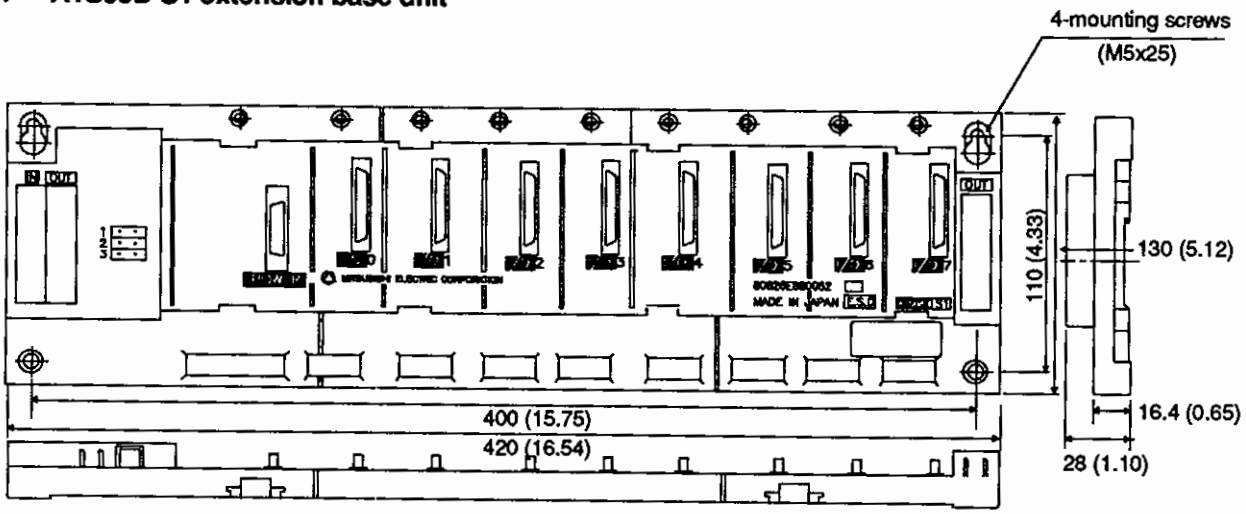
Unit: mm (in)

3.4.6 A1S65B-S1 extension base unit



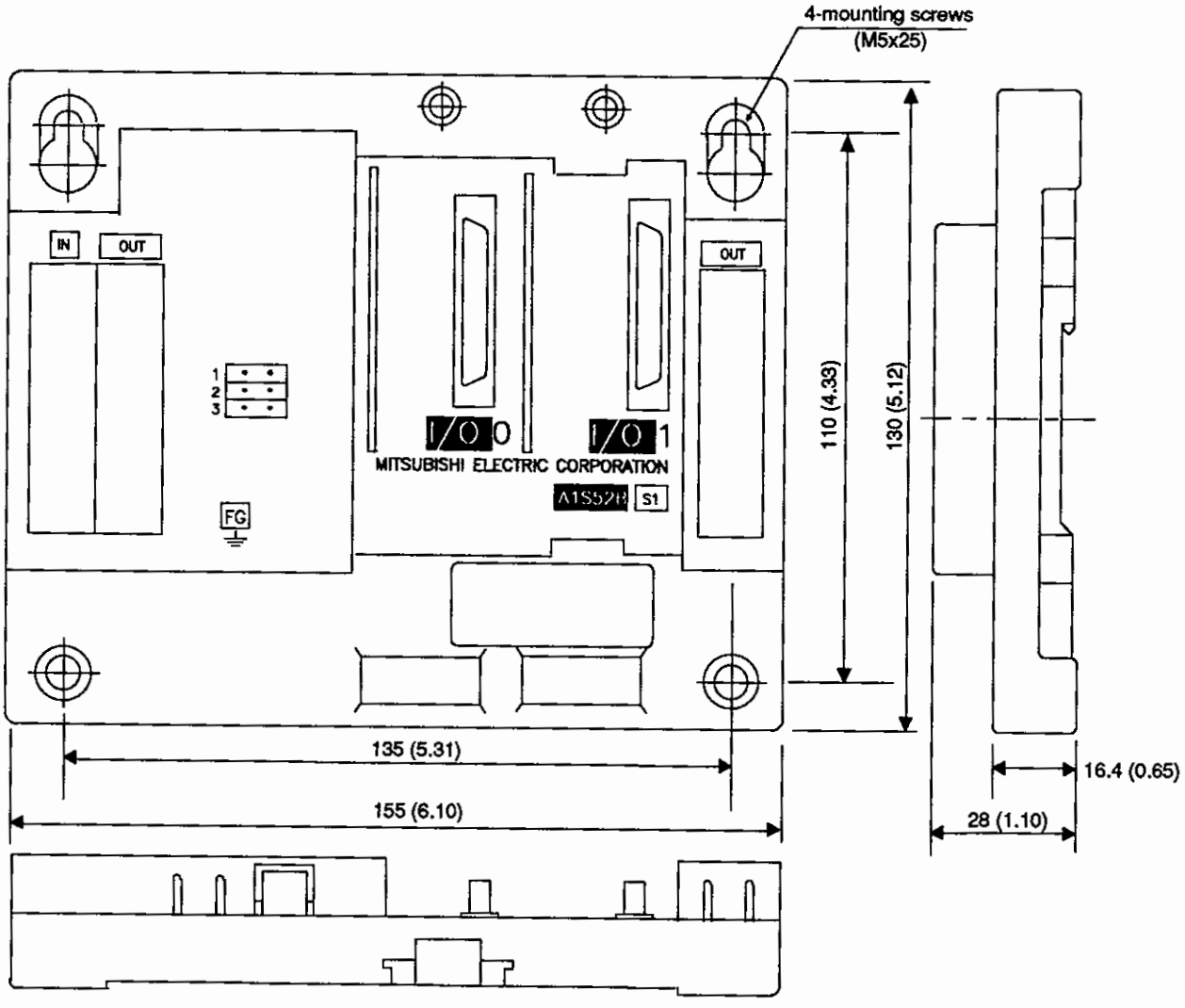
Unit: mm (in)

3.4.7 A1S68B-S1 extension base unit



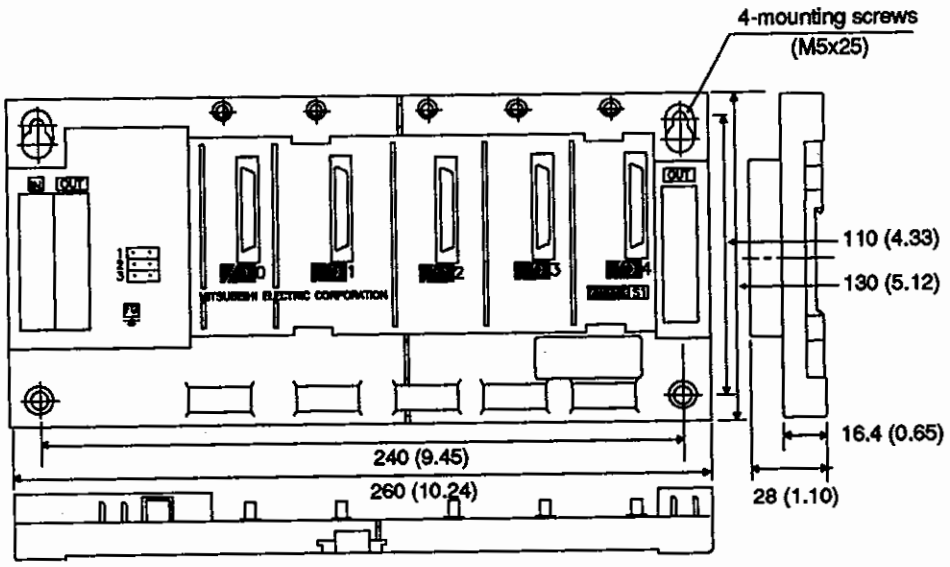
Unit: mm (in)

3.4.8 A1S52B-S1 extension base unit



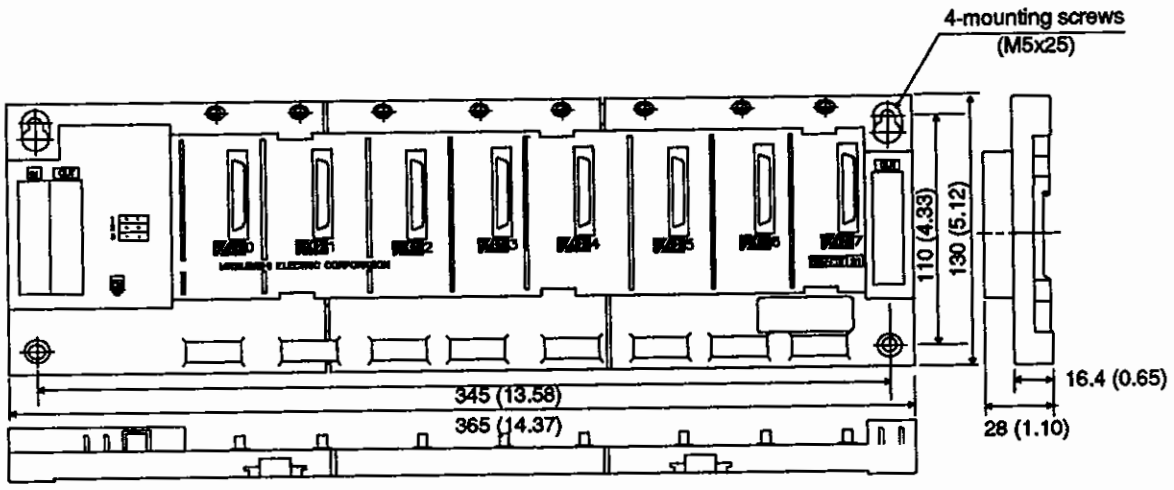
Unit: mm (in)

3.4.9 A1S55B-S1 extension base unit



Unit: mm (in)

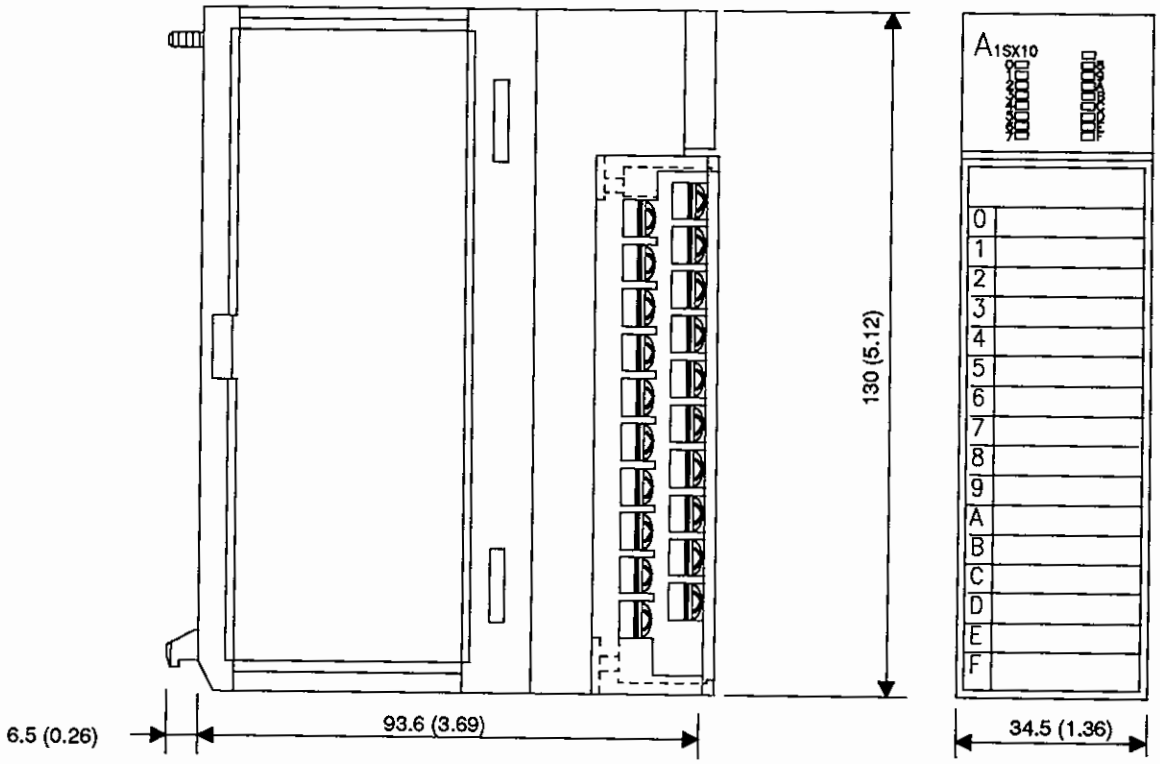
3.4.10 A1S58B-S1 extension base unit



Unit: mm (in)

3.5 Input/Output Modules

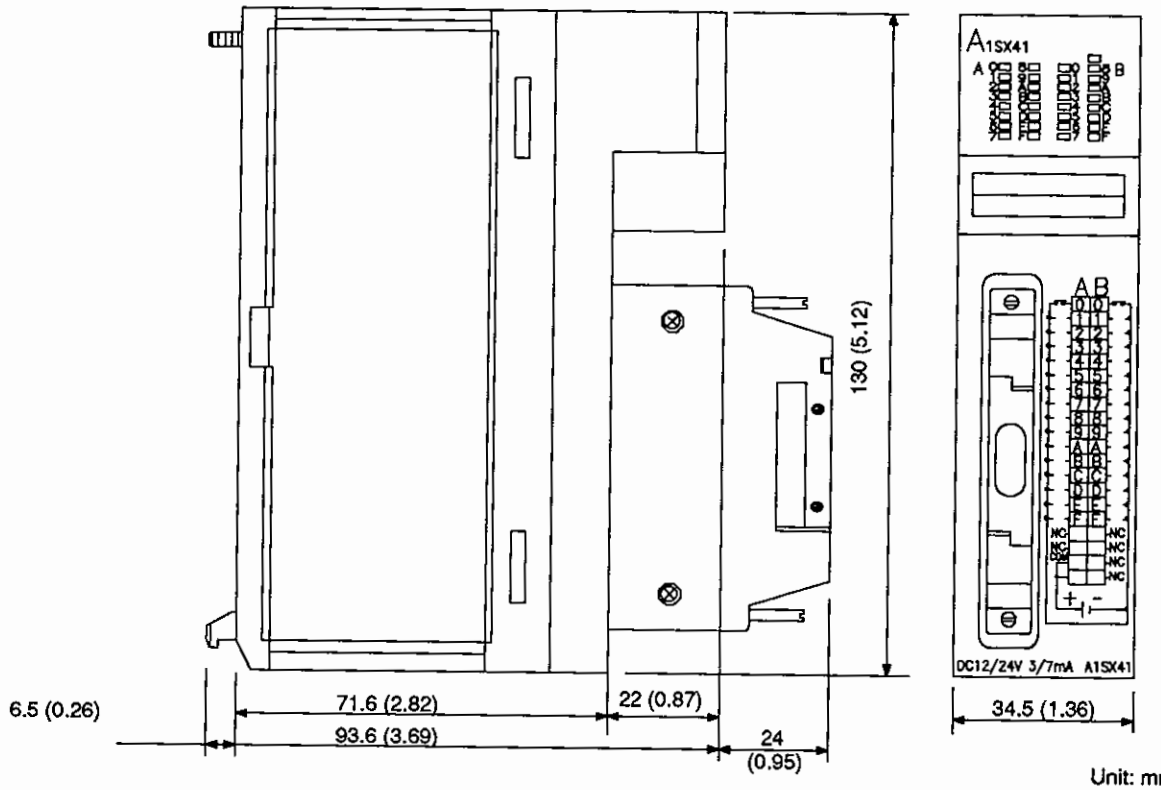
3.5.1 Terminal base connecting type



3.5.2 40-pin connector type

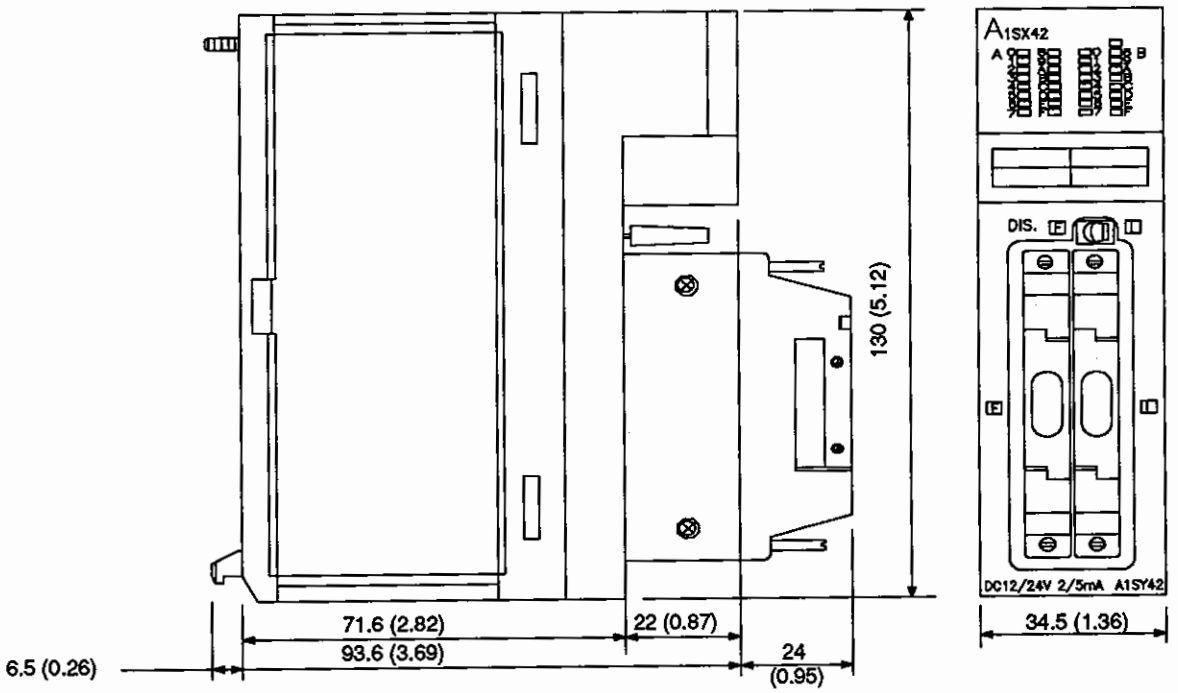
Unit: mm (in)

(1) 32-input/output module



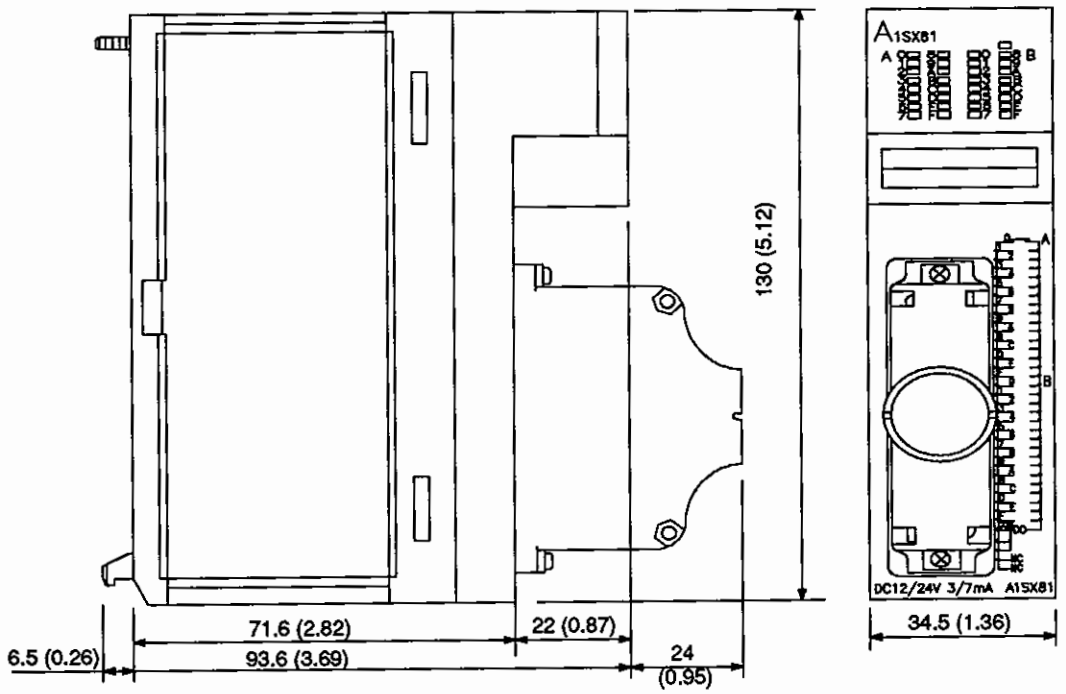
Unit: mm (in)

(2) 64-input/output module



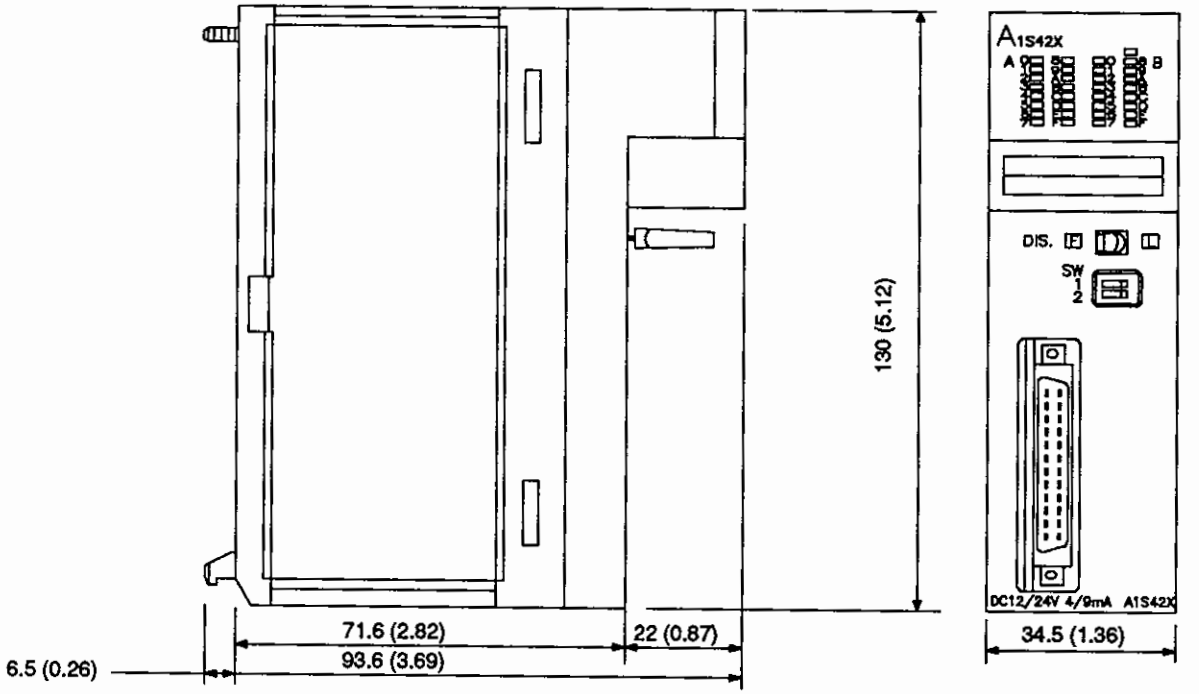
Unit: mm (in)

3.5.3 37-pin D sub-connector type 32-input/output module



Unit: mm (in)

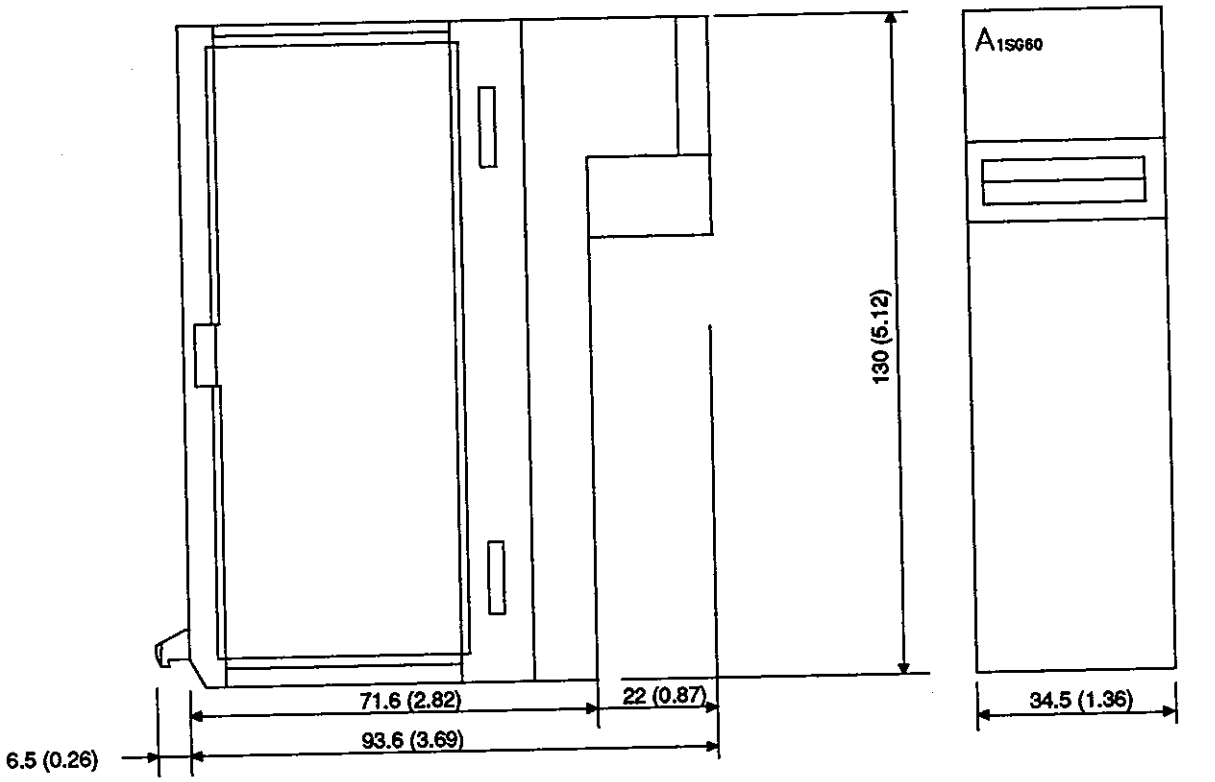
3.5.4 Dynamic I/O module



Unit: mm (in)

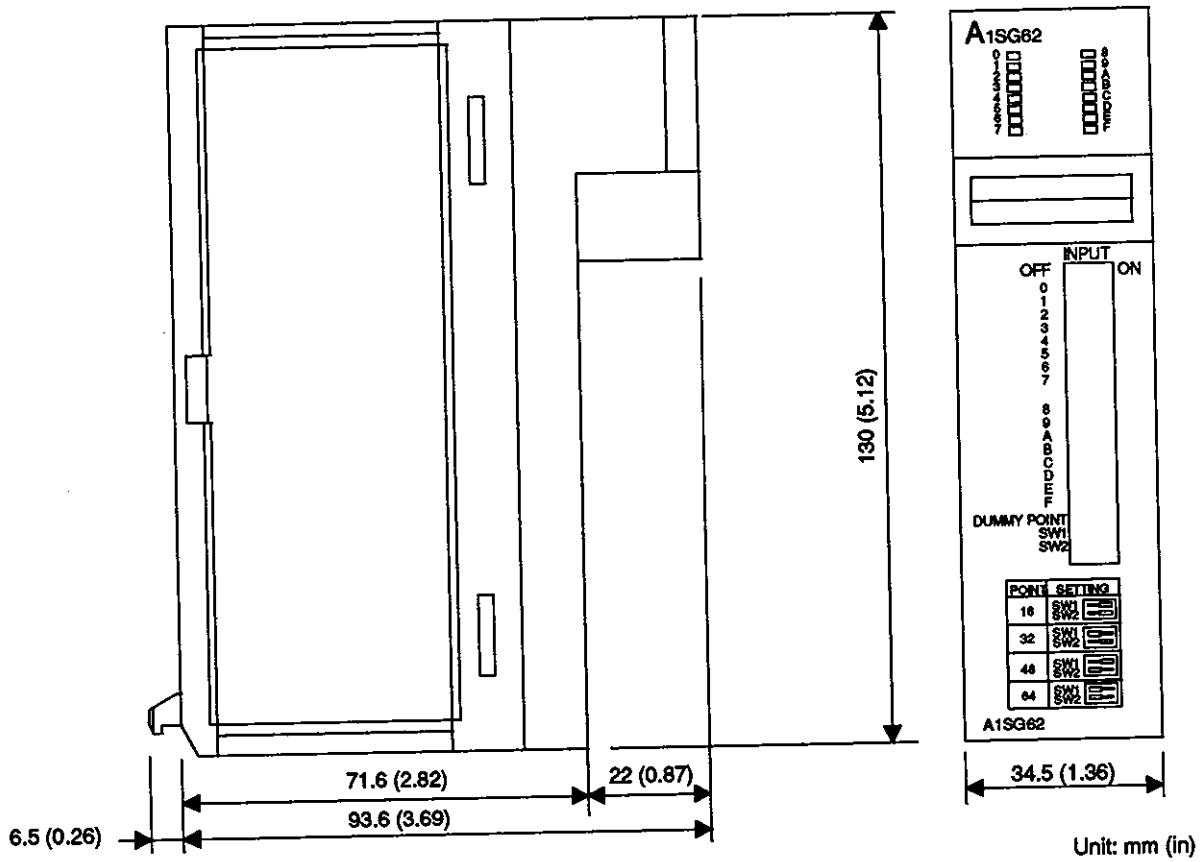
3.6 Dummy Module, Blank Cover

3.6.1 A1SG60 blank cover



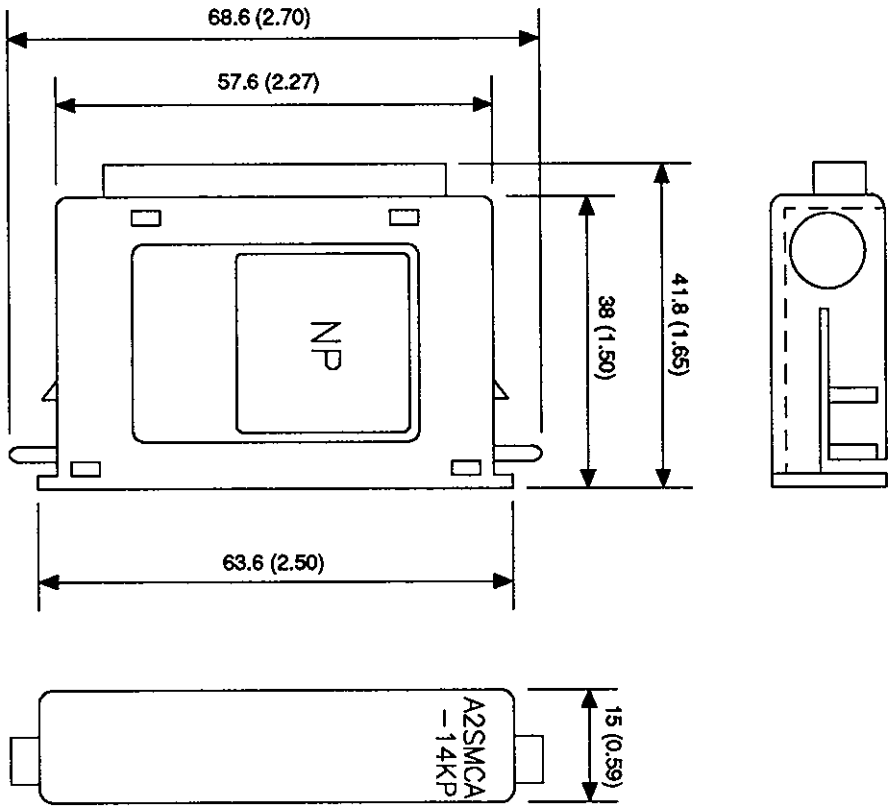
Unit: mm (in)

3.6.2 A1SG62 dummy module



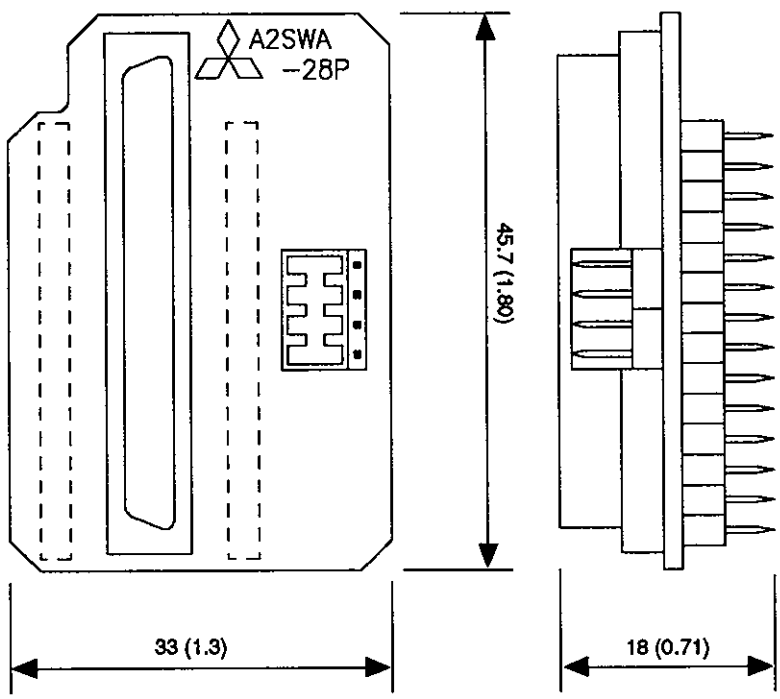
Unit: mm (in)

3.7 Memory Cassette (A2SMCA-[ ])



Unit: mm (inch)

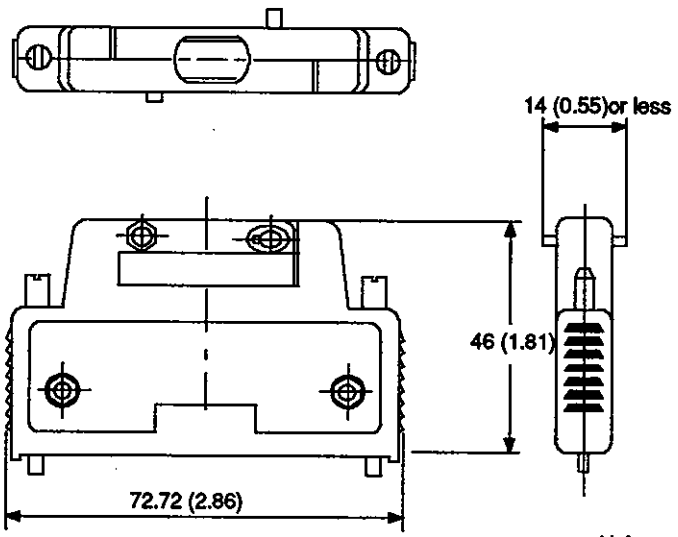
3.8 A2SWA-28P Memory Write Adaptor



Unit: mm (inch)

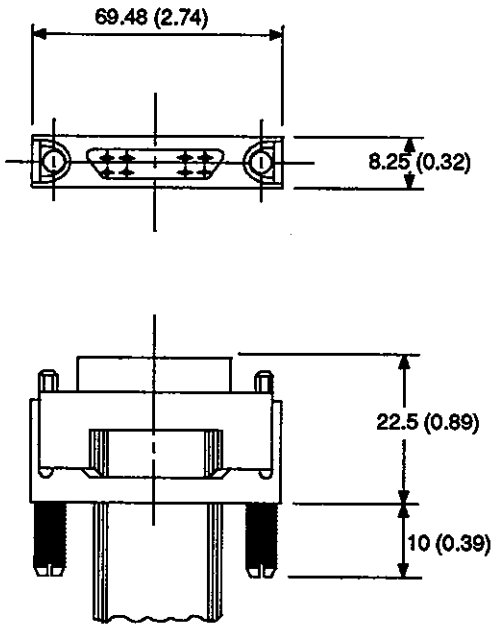
3.9 40-pin Connectors

3.9.1 A6CON1 soldering-type 40-pin connector, A6CON2 crimp-contact-type 40-pin connector



Unit: mm (inch)

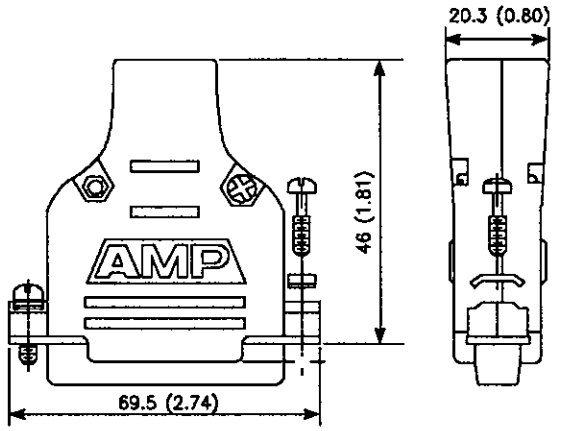
3.9.2 A6CON3 pressure-displacement-type 40-pin connector



Unit: mm (inch)

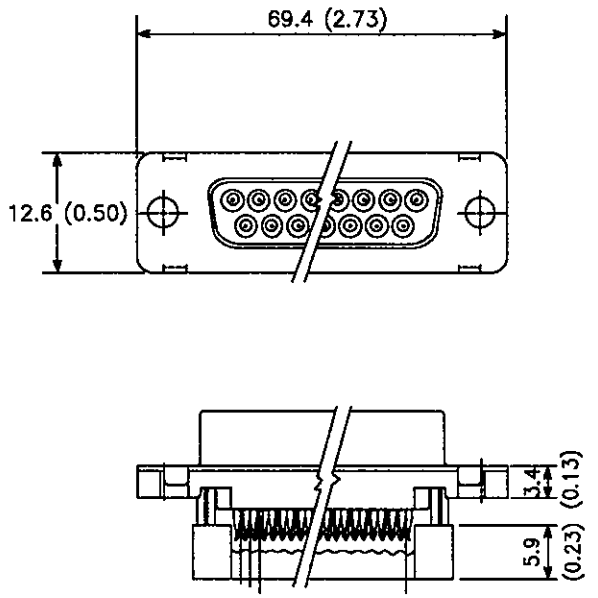
3.10 37-pin D sub-connectors

3.10.1 A6CON1E soldering type 37-pin D sub-connector
A6CON2E crimp-contact-type 37-pin D sub-connector



Unit: mm (inch)

3.10.2 A6CON3E pressure-displacement-type 37-pin D sub-connector



Unit: mm (inch)

IMPORTANT

(1) Design the configuration of a system to provide an external protective or safety inter locking circuit for the PCs.

(2) The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.

(a) Ground your body and the work bench.

(b) Do not touch the conductive areas of the printed circuit board and its electrical parts with non-grounded tools, etc.

Under no circumstances will Mitsubishi Electric be liable or responsible for any consequential damage that may arise as a result of the installation or use of this equipment.

All examples and diagrams shown in this manual are intended only as an aid to understanding the text, not to guarantee operation. Mitsubishi Electric will accept no responsibility for actual use of the product based on these illustrative examples.

Owing to the very great variety in possible applications of this equipment, you must satisfy yourself as to its suitability for your specific application.

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